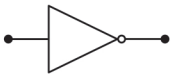
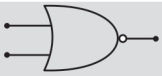
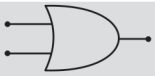
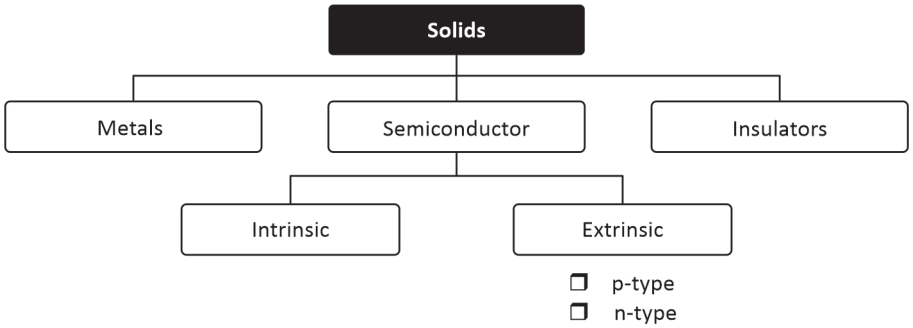
Semiconductor

Materials, Devices and Simple Circuits

Circuit Elements and Symbols :

Element	Symbol	Element	Symbol	Element	Symbol
PN - junction diode		AND gate		Zener diode	
NOT gate		n-p-n transistor		NAND gate	
p-n-p transistor		NOR gate		OR gate	



Basic Definitions :

1. **Energy Bands:** Inside the crystal, each electron has a unique position and no two electrons see exactly the same pattern of surrounding charges. Because of this, each electron will have different energy level. These different energy levels with continuous energy variation from what are called energy bands.

   OR

   Inside the crystal, each electron has a different energy level. These different energy levels with continuous energy variation from what are called energy bands.

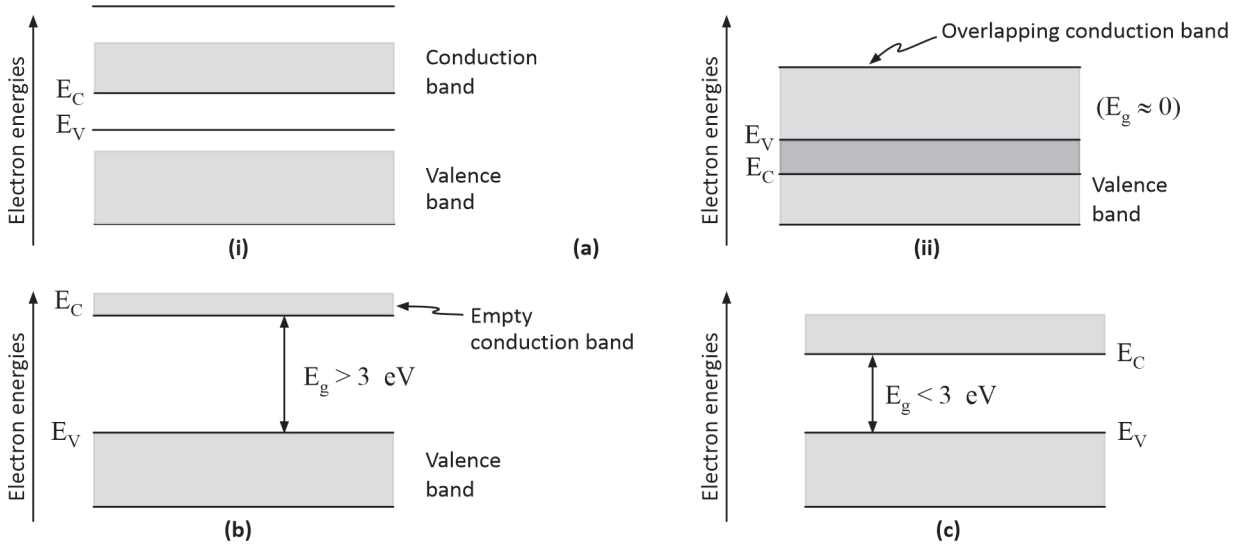
2. **Valence Band:** The energy band which includes the energy levels of the valence electrons is called the valence band.

3. **Conduction Band:** The energy band above the valence band is called the conduction band.

4. **Energy Band Gap:** The gap between the top of the valence band and bottom of the conduction band is called the energy band gap (Energy gap : Eg). It may be large, small or zero, depending upon the material.

Classification of Metals, Insulators and Semiconductors

	Metals	Semiconductors	Insulators
On the basis of conduction	The possess very low resistivity (or high conductivity)	They have resistivity or conductivity intermediate to metals and insulators	They have high resistivity (or low conductivity)
On the basis of energy bands	In metals, either the conduction band is partially filled and the valence band is partially empty or the conduction and valence bands overlap. When there is overlap, electrons from valence band can easily move into the conduction band making large number of electrons available for electrical conduction. When the valence band is partially empty, electrons from its lower level can move to higher level making conduction possible. Therefore, the resistance of such materials is low or the conductivity is high.	In this case, a finite but small band gap ($E_g < 3eV$) exists. Because of the small band gap, at room temperature some electrons from valence band can acquire enough energy to cross the energy gap and enter the conduction band. These electrons (though small in number) can move in the conduction band. Hence the resistance of semiconductors is not as high as that of the insulators.	In the case of insulators, a large band gap E_g exists ($E_g > 3eV$). There are no electrons in the conduction band and the energy gap is so large that electrons cannot be excited from the valence band to the conduction band thermal excitation. Therefore, no electrical conduction is possible.

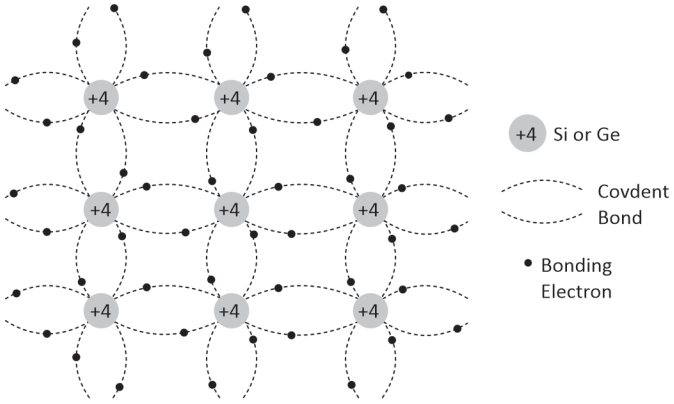


Difference between energy bands of (a) metals, (b) insulators and (c) semiconductors.

Intrinsic Semiconductor :

Definition : A semiconductor in an extremely pure form (free from all impurities) is known as an intrinsic semiconductor. Germanium and silicon are the commonly used semiconductors

- Let us take the common case of Si and Ge. We know that Si and Ge have four valence electrons. In its crystalline structure, every Si or Ge atom tends to share one of its four valence electrons with each of its four nearest neighbor atoms, and also to take share of one electron from each such neighbor. Such a situation arises at low temperature.

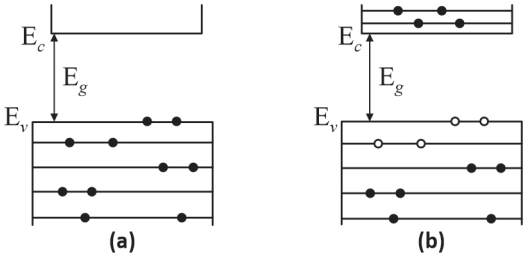


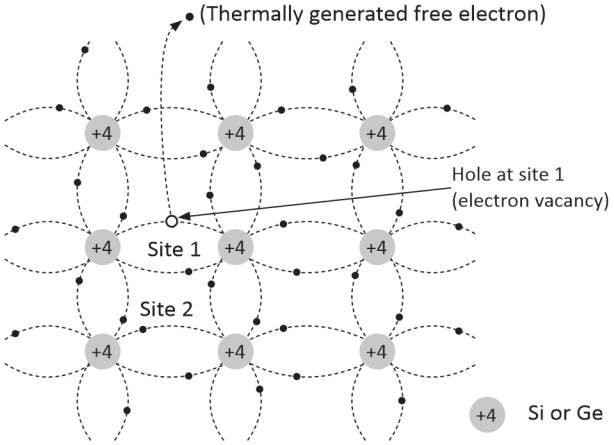
Schematic two-dimensional representation of Si or Ge structure showing covalent bonds at low temperature (all bonds intact). + 4 symbol indicates inner cores of Si or Ge

An intensive semiconductor at

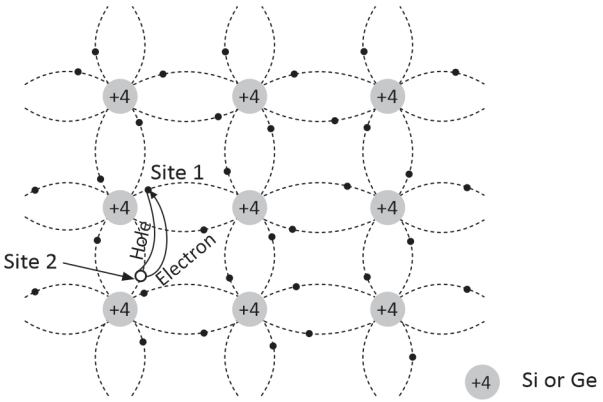
(a) T = 0K **(b)** T > 0K

$\left[\begin{array}{l} \bullet \equiv \ \bar{e} \\ \circ \equiv \ \text{holes} \end{array}\right]$





Schematic model of generation of hole at site 1 and conduction electron due to thermal energy at moderate temperatures.



Simplified representation of possible thermal motion of a hole. The electron from the lower left hand covalent bond (site 2) goes to the earlier hole site 1, leaving a hole at its site indicating an apparent movement of the hole from site 1 to site 2.

➤ As the temperature increases, more thermal energy becomes available to these and the electrons may break-away (become free electrons contributing to conduction).

The neighbourhood, from which the free electron (with charge $-e$) has come out leaves a vacancy with an effective charge ($+e$). This vacancy with the effective positive electronic charge is called a <u>hole</u>.

<u>The hole behaves as an apparent free particle with effective positive charge.</u>

➤ In intrinsic semiconductors, the number of free electrons (n_e) is equal to the number of hole (n_h)
i.e. $n_e = n_h = n_i$ where n_i is called intrinsic carrier concentration.

➤ Under the action of an electric field, the free electron moves completely independently as conduction electron giving rise to an electron current (I_e) and the holes move towards negative potential giving the hole current (I_h).

Thus, the total current (I) is the sum of the electrons current (I_e) and the hole current (I_h) i.e. $I = I_e + I_h$

Note : Apart from the process of generation of conduction electrons and holes, a simultaneous process of recombination occurs in which the electrons recombine with the holes.

At equilibrium, the rate of generation is equal to the rate of recombination of charge carriers. The recombination occurs due to an electron colliding with a hole.

Limitations of Intrinsic Semiconductor :

(i) The number of intrinsic charge carriers (holes and electrons) is very small. Hence, these are low conducting materials.

(ii) Not enough flexibility is available in controlling the number of intrinsic charge carriers as they are thermally generated.

Extrinsic Semiconductor :

Definitions :

(i) Extrinsic Semiconductor : When a small amount of a suitable impurity is added to the pure semiconductor, the conductivity of the semiconductor is increased manifold. Such materials are known as extrinsic semiconductors or impurity semiconductors.

OR

A semiconductor doped with a suitable impurity, so as to possess conductivity much higher than the semiconductor in pure form is called an extrinsic semiconductor.

(ii) Doping : The deliberate addition of a desirable impurity to an intrinsic semiconductor to increase its conductivity is called doping.

(iii) Dopants : The impurity atoms added to an intrinsic semiconductor to increase its conductivity are called dopants.

Necessary Condition for Doping :

The dopant has to be such that it does not distort the original pure semiconductor lattice. In other words, the sizes of the dopant and the semiconductor atoms should be nearly the same.

There are Two types of Dopants used in Doping the Tetravalent Si or Ge :

(i) Pentavalent (valency 5) : Like Arsenic (As), Antimony (Sb), Phosphorus (P), etc.

(ii) Trivalent (valency 3) : Like Indium (In), Boron (B), Aluminium (Al). etc.

❒ n-Type Semiconductor

➤ When an atom of +5 valency element occupies the position of an atom in the crystal lattice of Si, four of its electrons bond with the four silicon neighbours while the fifth remains very weakly bound to its parent atom.

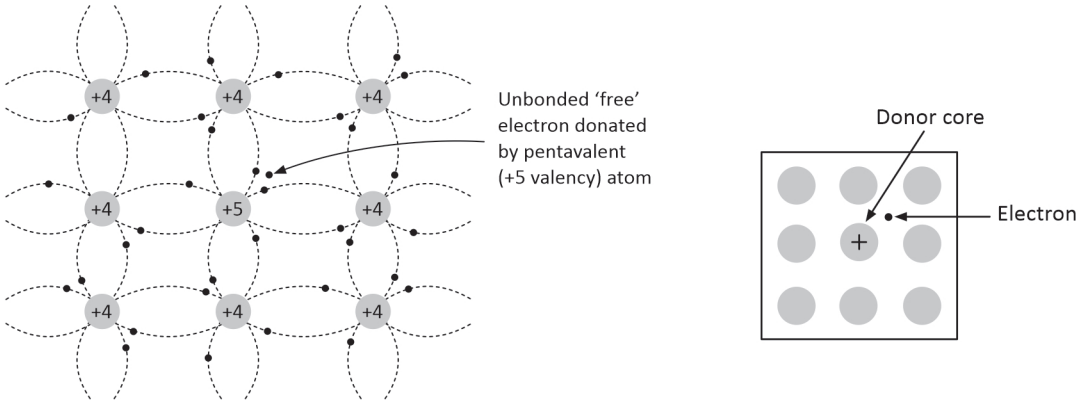
➤ This is because the four electrons participating in bonding are seen as part of the effective core of the atom by the fifth electron. As a result, the ionization energy required to set this electron free is very small and even at room temperature, it will be free to move in the lattice of the semiconductor.

- Thus, the pentavalent dopant is donating one extra electron for conduction and hence is known as donor impurity.
- The number of electrons made available for conduction by dopant atoms depends strongly upon the doping level and is independent of any increase in ambient temperature.

  On the other hand, the number of free electrons (with an equal number of holes) generated by Si atoms, increases weakly with temperature.
- In a doped semiconductor, the total number of conduction electrons (n_e) is due to the electrons contributed by donors and those generated intrinsically, while the total no. of holes (n_h) is only due to the holes from the intrinsic source. But the rate of recombination of holes would increase due to the increase in the number of electrons. As a result, the number of holes would get reduced further.
- Hence, in an extrinsic semiconductor doped with pentavalent impurity, electrons are the majority carriers and holes the minority carriers.

These semiconductors are, therefore, known as *n*-type semiconductors.

For *n*-type semiconductors, $n_e >> n_h$



(a) Pentavalent donor atom (As, Sb, P, etc). doped for tetravalent Si or Ge giving n-type semiconductor, and
(b) Commonly used schematic representation of n-type material which shows only the fixed cores of the substituent donors with one additional effective positive charge and its associated extra electron

❒ **p-Type Semiconductor :** This is obtained when Si or Ge is doped with a trivalent impurity like Al, B, In, etc.

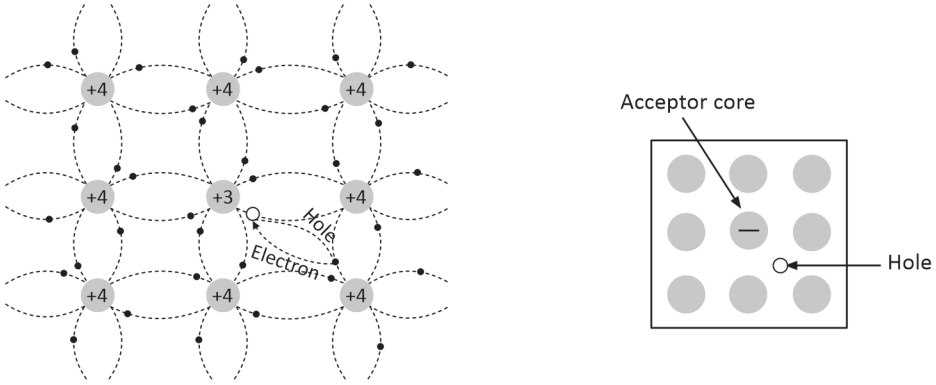
The dopant has one valence electron less than Si or Ge and, therefore, this atom can form covalent bonds with neighboring three Si atoms but doesnot have any electron to offer to the fourth Si atom. So, the bond between the fourth neighbour and the trivalent atom has a vacancy or hole.

- To hold the dopant atom tightly within Si or Ge, some of the outer bound electrons in the neighbourhood may jump to fill this vacancy, leaving a vacancy or hold at its own site. Thus, the hole is available for conduction.
- The trivalent foreign atom becomes effectively negatively charged when it shares fourth electron with neighboring Si atom.

  Therefore, the dopant atom of *p*-type material can be treated as core of one negative charge along with its associated hole.

➤ The holes are both due to acceptor atoms as well as intrinsically generated while the source of conduction electrons is only intrinsic generation. Thus, holes are the majority carriers and electrons are minority carriers.

Here, $n_h >> n_e$



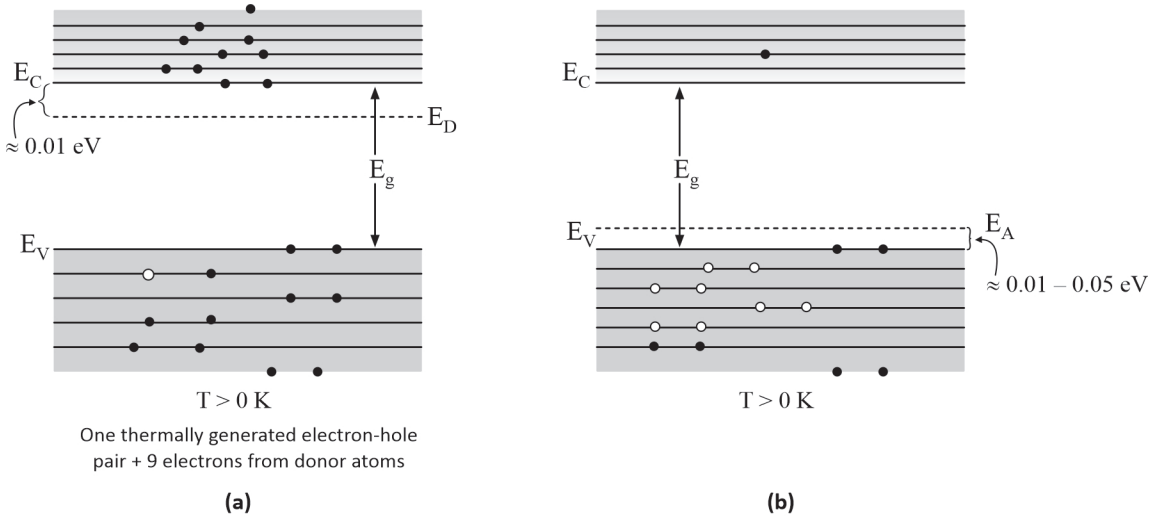
(a) Trivalent acceptor atom (In, Al, B etc.) doped in tetravalent Si or Ge lattice giving p-type semiconductor.
(b) Commonly used schematic representation of p-type material which shows only the fixed core of the substituent acceptor with one effective additional negative charge and its associated hole.

Description on the Basis of Energy Bands :

(i) n-Type Semiconductor :

➤ The donor energy level E_D is slightly below the bottom E_C of the conduction band and electrons from this level move into the conduction band with very small supply of energy.

At room temp., most of the doner atoms get ionized but very few Si atoms get ionized. So, the conduction band will have most electrons coming from the donor impurities.



Energy bands of **(a)** n - type semiconductor at T > 0 K **(b)** p-type semiconductor at T > 0 K

(ii) p-Type Semiconductor :

- The acceptor energy level E_A is slightly above the top E_V of the valence band.
- With very small supply of energy, an electron from the valence band can jump to the level E_A and ionize the acceptor negatively. Or we can say that with very small supply of energy, hole from E_A sinks down into valence band.
- At room temperature, most of the acceptor atoms get ionized leaving holes in the valence bond. Thus, at room temperature, the density of holes in the valence band is predominantly due to impurity in the extrinsic semiconductor.

Note : Even after doping, the crystal maintains an overall charge neutrality as the charge of additional charge carriers is just equal and opposite to that of the ionized cores in the lattice.

The $\bar{e}$ and hole concentration in thermal equilibrium is always given by:

$$\boxed{n_e n_h = n_i^2}$$

Illustration 1

An intrinsic sample of germanium crystal has a hole of 10^{13} cm^{-3} at the room temperature. When doped with antimony the hole density is decreased to 10^{11}cm^{-3} at the same temperature. Find the number density of majority charge carriers.

SOLUTION :

We know that $n_e n_h = n_i^2$ $\therefore$ $n_e = \dfrac{n_i^2}{n_h}$

$$= \frac{(10^{13})^2}{10^{11}} = 10^{15}\ cm^{-3}$$

Illustration 2

Find the current produced at a room temperature in a pure germanium plate of area 2×10^{-4} m^2 and of thickness 1.2×10^{-3} m when a potential of 5V is applied across the faces. Concentration of carries in germanium at room temperature is 1.6×10^6 per cubic metre. The mobilities of electrons and holes are 0.4 m^2 V^{-1} s^{-1} and 0.4 m^2 V^{-1} s^{-1} respectively. How much heat is generated in the plate in 100 second ?

SOLUTION :

Electric field $E = \dfrac{V}{d} = \dfrac{5}{1.2\times10^{-3}} = \dfrac{5}{12}\times10^4 V/m$

Electric current across the plate : We know that $\mu = \dfrac{v_d}{E}$ $\therefore$ $v_d = \mu E$

Thus $i = neAE\mu = neAE\,(\mu_e + \mu_h)$

$$= 1.6\times10^6 \times 1.6\times10^{-19} \times 2\times10^{-4} \times \frac{5}{12}\times10^4 \times 2(0.4+0.2)$$

$= 1.28 \times 10^{-13}$ A

Heat produced in the plate in 100 second

$H = Vit = 5 \times 1.25 \times 10^{-13} \times 100 = 6.4 \times 10^{-11}$ J.

Illustration 3

If resistivity of pure silicon is 3000 ohm-metre and the mobilities of electrons and holes are 0.12 m^2/V-s and 0.025 m^2/V-s respectivey, find :

(i) the resistivity of a specimen of the material when 10^{19} atoms of phosphorus are added per ms.

(ii) the resistivity of specimen if further 2×10^{19} boron atoms per m^3 are also added.

SOLUTION :

The resisitivity of semiconductor is given by $\rho = \frac{1}{\sigma} = \frac{1}{n_i e(\mu_e + \mu_h)}$

$$\therefore \quad n_i = \frac{1}{\rho e(\mu_e + \mu_h)} = \frac{1}{3000 \times 1.6 \times 10^{-19}(0.12 + 0.025)} = 1.437 \times 10^{16} m^{-3}$$

(i) When 10^{19} atoms of phosphorus (donor atoms) are added per m^3, we have $n_e >> n_h$

$$\therefore \quad \rho = \frac{1}{n_e e \mu_e} = \frac{1}{10^{19} \times 1.6 \times 10^{-19} \times 0.12} = 5.21 \text{ ohm-m}$$

(ii) When 2×10^{19} boron (acceptor atoms) are also added, we have

$$n_h - n_e = n_{\text{acceptor}} - n_{\text{donor}} = 2 \times 10^{19} - 10^{19}$$

Since $n_h > h_e$, hence $n_h \simeq 10^{19}$

$$\therefore \quad \rho = \frac{1}{n_h e \mu_h} = \frac{1}{10^{19} \times 1.6 \times 10^{-19} \times 0.025} = 25 \text{ ohm-m}$$

p-n Junction :

Definition: The device obtained by growing a p-type semiconductor over a n-type semiconductor or vice-versa is called a p-n junction. It is also called a junction diode

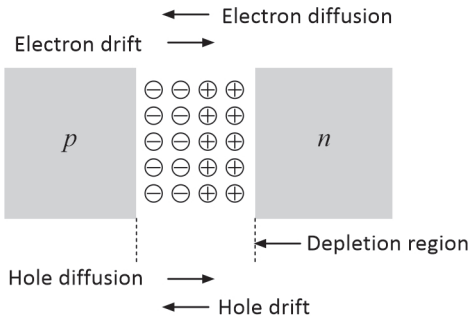
OR

A p-n junction is an atomic layer of separation between a p-type and an n-type semiconductor.

p-n Junction Formation :

Two processes occur during the formation of a p-n junction :

(i) Diffusion **(ii)** Drift



p-n Junction formation process

❒ **Diffusion :**

- ➤ In an n-type semiconductor,

  (Concentration of electrons) > (Concentration of holes)

- ➤ Similarly, in a p-type semiconductor,

  (Concentration of hole) > (Concentration of electrons)

- ➤ During the formation of p-n junction, and due to the concentration gradient across p – and n – sides, holes diffuse from p-side to n-side (p → n) and electrons diffuse from n-side to p-side (n → p).
- ➤ This motion of charge carriers give rise to diffusion current across the junction.

❒ When an electron diffuses from n → p, it leaves behind an ionized donor on n-side.

This ionized donor (positive charge) is immobile as it is bonded to the surrounding atoms.

As the electrons continue to diffuse from n → p, a layer of positive charge (or positive space-charge region) on n-side of the junction is developed.

❒ Similarly, when a hole diffuses from p → n due to the concentration gradient, it leaves behind an ionized acceptor (negative charge) which is immobile.

As the holes continue to diffuse, a layer of negative charge (or negative space – charge region) on the p-side of the junction is developed.

❒ This space-charge region on either side of the junction together is known as depletion region as the electrons and holes taking part in the initial movement across the junction depleted the region of its free charges.

❒ **Drift :**

- ➤ Due to the positive space-charge region on n-side of the junction and negative space-charge region on p-side of the junction, an electric field directed from positive charge towards negative charge develops.
- ➤ Due to this field, an electron on p-side of the junction moves to n-side and a hole on n-side of the junction moves to p-side.
- ➤ The motion of charge carriers due to the electric field is called drift.

  Thus, a drift current, which is opposite in direction to the diffusion current starts.

- ➤ Initially, diffusion current is large and drift current is small.

As the diffusion process continues, the space – charge regions on either side of the junction extend, thus increasing the electric field strength and hence drift current.

This process continues until the diffusion current equals the drift current. Thus, a p-n junction is formed.

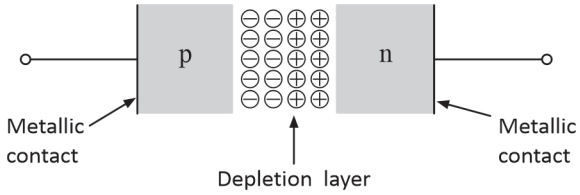
Note **:** In a p-n junction under equilibrium, there is *no net current*.

Barrier Potential :

- ➤ The loss of electrons from the n-region and the gain of electrons by the p-region causes a difference of potential across the junction of the two regions.
- ➤ The polarity of this potential is such as to oppose further flow of carriers so that a condition of equilibrium exists.
- ➤ Since this potential tends to prevent the movement of electron from the n-region into the p-region, it is often called a barrier potential.

Semiconductor Diode :

A semiconductor diode is basically a p-n junction with metallic contacts provided at the ends for the application of an external voltage. It is a two-terminal device.



Semiconductor diode

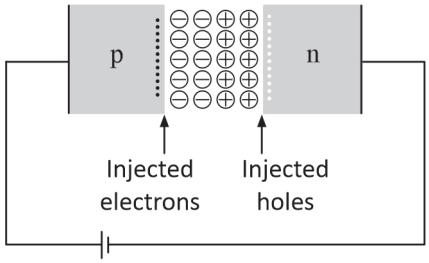
IDEAL DIODE: One which allows current to pass completely in forward bias and no current to pass in reverse bias.

➤ p-n Junction Diode under forward Bias :

The p-n junction diode is said to be forward bias if p-side of the junction is connected to the positive terminal of the battery and n-side to the negative terminal i.e. the direction of the applied voltage (V) is opposite to the built-in potential (V_0).

❒ Consequences :

- ➤ The depletion layer width decreases.
- ➤ The barrier height is reduced. The effective barrier height under forward bias is ($V_0 - V$).
- ➤ Due to the applied voltage, electrons from n-side cross the depletion region and reach p-side (where they are minority carriers).



Forward bias minority carrier injection

Similarly, holes from p-side cross the junction and reach the n-side (where they are minority carriers).

This process under forward bias is known as minority carrier injection.

- ➤ At the junction boundary, on each side, the minority carrier concentration increases significantly compared to the locations far from the junction.
- ➤ Due to this concentration gradient, the injected electrons on p-side diffuse from the junction edge of p-side to the other end of p-side.
- ➤ Likewise, the injected holes on n-side diffuse from the junction edge of n-side to the other end of n-side.
- ➤ This motion of charged carriers on either side gives rise to current.

The total diode forward current is sum of hole diffusion current and conventional current due to electron diffusion. The magnitude of this current is usually in mA.

- ➤ The applied voltage mostly drops across the depletion region & the voltage drop across n- side and p-side is negligible (this is because resistance of depletion region ; a region where there are no charges ; is very high as compared to n & p sides.)

➤ p-n junction diode under reverse bias :

A p-n junction diode is said to be reverse biased if n-side is connected to the positive terminal of the battery and p-side to the negative terminal i.e. the direction of the applied voltage is same as the direction of barrier potential.

Here also applied voltage drops across depletion region.

❒ Consequences:

- The depletion region widens.
- The barrier height increases. The effective barrier height under reverse bias is $(V_0 + V)$
- This suppresses the flow of electrons from $n \rightarrow p$ and holes from $p \rightarrow n$. Thus, diffusion current, decreases enormously compared to the diode under forward bias.
- The electric field direction of the junction is such that if electrons on p-side in their random motion come close to the junction, they will be swept to its majority zone.

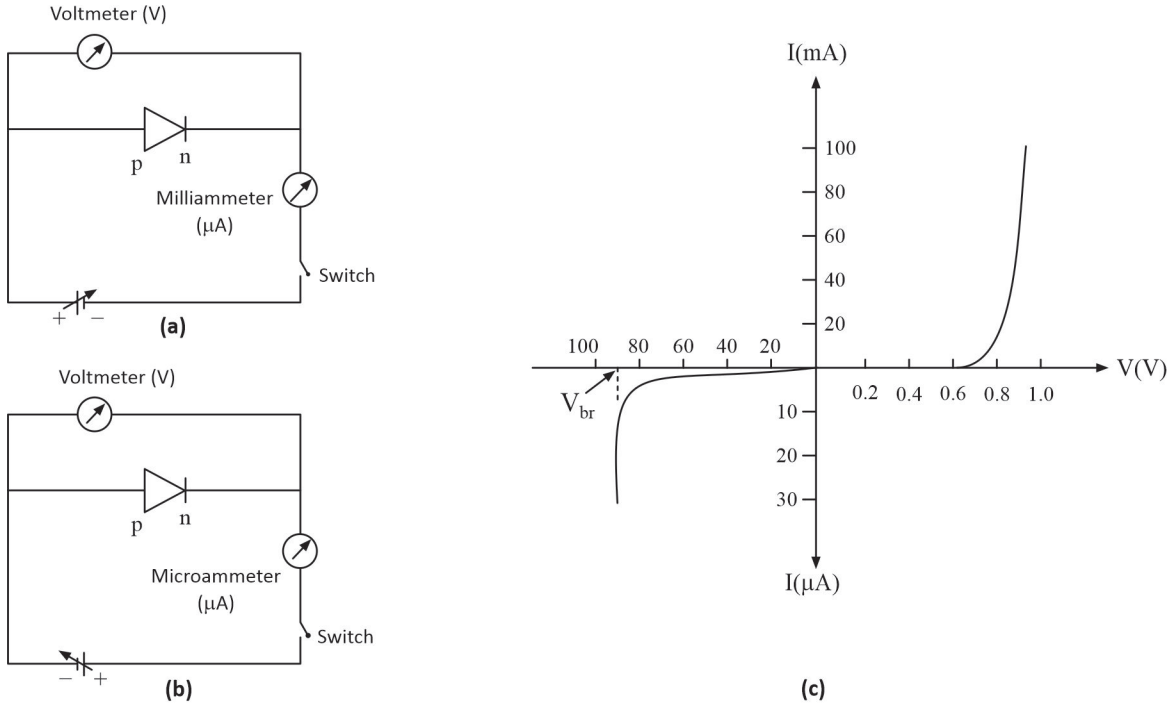
  This drift of carriers gives rise to current.
- The drift current is quite low (of the order of a few μA) because it is due to the motion of carriers from their minority side to their majority side across the junction.
- The diode reverse current is not very much dependent on the applied voltage. Even a small voltage is sufficient to sweep the minority carriers from one side of the junction to the other side of junction.
- The current is not limited by the magnitude of the applied voltage but is limited due to the concentration of the minority carrier on either side of the junction.

V-I Characteristic of p-n Junction Diode :

Dynamic Resistance : It is defined as the ratio of small change in voltage ΔV to a small change in current ΔI.

$$r_d = \frac{\Delta V}{\Delta I}$$

Forward Characteristics :



Experimental circuit arrangement for studying V-I characteristics of a p-n junction diode
(a) in forward bias, **(b)** in reverse bias and **(c)** Typical V-I characteristics of a silicon diode

- In forward bias, the current increases very slowly, almost negligibly, till the voltage across the diode crosses a certain value.
- After the characteristic voltage, the diode current increases significantly (exponentially), even for a very small increase in the diode bias voltage. This voltage is called the threshold voltage or cut-in voltage.

Reverse Characteristics :

- For the diode in reverse bias, the current is very small (~μA) and almost remains constant with change in bias. It is called *reverse saturation current*.
- A very high reverse bias (break down voltage) i.e. when $V = V_{br}$, the current increases sharply. Even a slight increase in the bias voltage causes large change in the current. (At Breakdown voltage, Si – Si bond starts breaking, thus large no. of free '*n*' & '*h*' such that *I* increase)

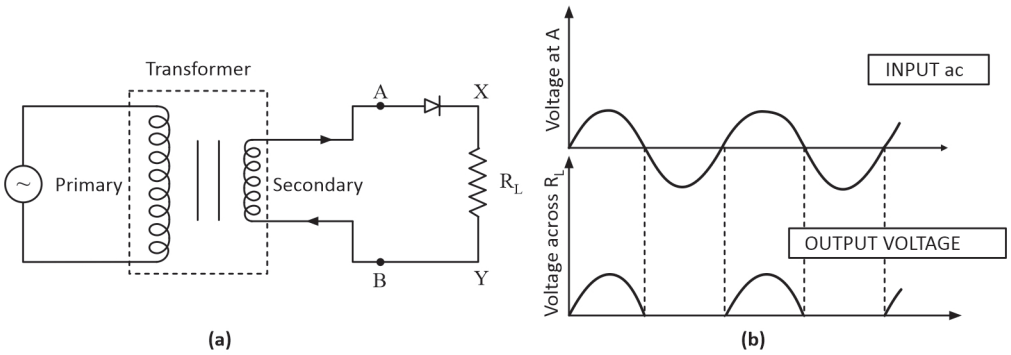
***Note*:** The p-n junction diode primarily allows the flow of current only in one direction (forward bias). The forward bias resistance is low as compared to the reverse bias resistance.

Application of Junction Diode as a Rectifier :

The p-n junction diode allows current to pass only when it is forward biased. So if an alternating voltage is applied across a diode, the current flows only in that part of the cycle when the diode is forward biased.

This property is used to rectify alternating voltage and the circuit used for this purpose is called a rectifier.

Half-Wave Rectifier :

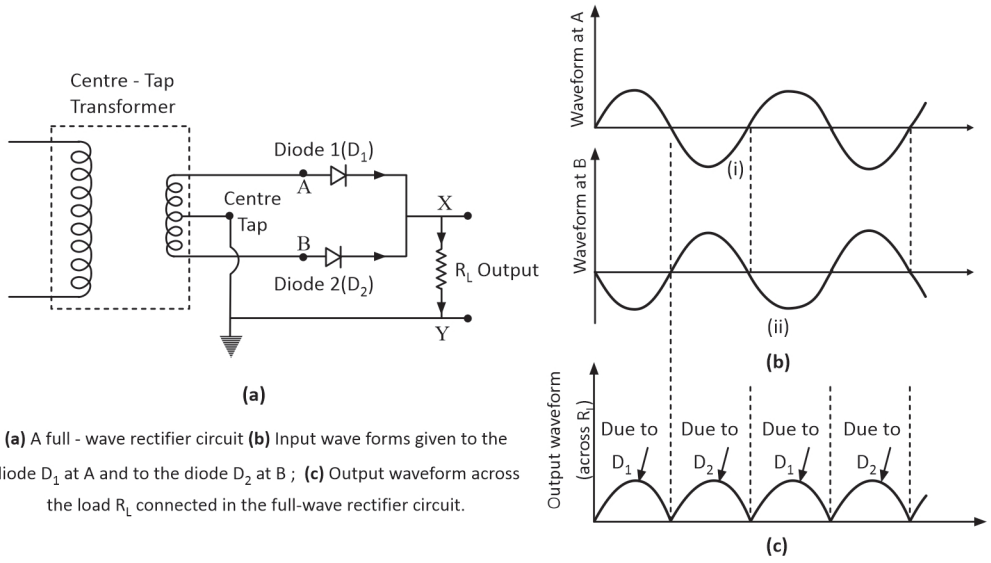


(a) Half - wave rectifier circuit, **(b)** Input ac voltage and output voltage waveforms from the rectifier circuit.

- When the voltage at A is positive, the diode is forward biased and it conducts.
- When A is negative, the diode is reverse-biased and it does not conduct.
- Therefore, in the positive half-cycle of ac there is a current through the load resistor R_L and we get an output voltage, whereas there is no current in the negative half-cycle.
- In the next positive half-cycle, again we get the output voltage.
- Thus, the output voltage, though still varying (pulsating), is restricted to only one direction and is said to be rectified.
- Since, the rectified output of this circuit is only for half of the input ac wave, it is called as half-wave rectifier.

***Note* :** The reverse breakdown voltage of the diode must be sufficiently higher than the peak ac voltage at the secondary of the transformer to protect the diode from reverse breakdown.

Full-Wave Rectifier :



(a) A full - wave rectifier circuit **(b)** Input wave forms given to the diode D_1 at A and to the diode D_2 at B ; **(c)** Output waveform across the load R_L connected in the full-wave rectifier circuit.

Construction :

- The p-side of the two diodes are connected to the ends of the secondary of the transformer.
- The n-side of the diodes are connected together and the output is taken between this common point of diodes and the midpoint of the secondary of the transformer.
- So, for a full-wave rectifier, the secondary of the transformer is provided with a centre tapping and so it is called centre-tap transformer.

Working :

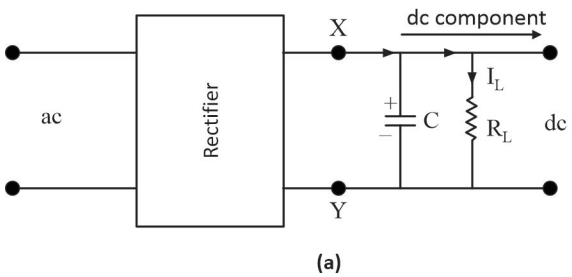
- The voltages at any instant at A (input of diode D_1) and B (input of diode D_2) with respect to the centre tap are out of phase with each other. (because at any instant, From $A \rightarrow B$, voltage is either increaing or decreasing i.e. Let voltage at A > B i.e. $V_A > V_P > V_B$ (V_P : centre tap) s.t. $V_A - V_P > 0 \Rightarrow D_1$ is Forward biased and $V_B - V_P < 0 \Rightarrow D_2$ is reverse biased. Similarly, when D_2 is forward biased D_1 will be reverse biased).
- Suppose the input voltage to A w.r.t. the centre tap at any instant is positive, then at that instant, voltage at B being out of phase will be negative.
- So, diode D_1 gets forward biased and conducts (while D_2 being reverse biased is not conducting.)
- Hence, during this positive half cycle we get an output current (and an output voltage across the load resistor R_L)
- In the course of the ac cycle when the voltage of A becomes negative w.r.t. centre tap, voltage at B would be positive.
- In this part of the cycle, diode D_1 would not conduct but diode D_2 would, giving an output current and output voltage (across R_L) during the negative half cycle of the input ac.
- Thus, we get output rectified voltage during both the positive as well as the negative half of the cycle and hence, it is known as full-wave rectifier.

Capacitor Filters :

- To get steady dc output from the pulsating voltage, normally a capacitor is connected across the output terminals (parallel to the load R_L). [One can also use an inductor in series with R_L for the same purpose].
- Since these additional circuits appear to filter out the ac ripple and give a pure dc voltage, so they are called filters.

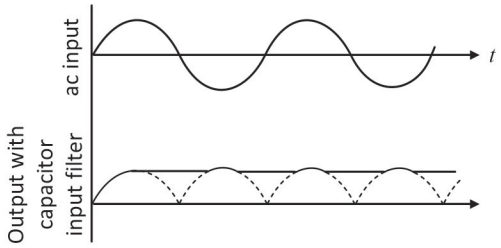
The Role of Capacitor in filtering :

- When the voltage across the capacitor is rising, it gets charged. If there is no external load, it remains charged to the peak voltage of the rectified output.
- When there is a load, it gets discharged through the load and the voltage across it begins to fall.
- In the next half cycle of rectified output, it again gets charged to the peak value.
- The rate of fall of voltage across the capacitor depends upon the inverse product of capacitor C and the effective resistance R_L used in the circuit and is called the time constant.



(a)

(a) A full-wave rectifier with capacitor filter.



(b)

(b) Input and output voltage of rectifier in (a).

Rate of fall of voltage across $c \propto \frac{1}{r} = \frac{1}{CR_L}$.

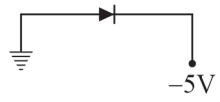
As τ increases, It takes longer for 'v' to fall (discharge) & by the time it starts falling, next cycle of current comes and thus graph is approx const.

To make the time constant large, value of C should be large. So, capacitor input filters use large capacitors.

- The output voltage obtained by using capacitor input filter is nearer to the peak voltage of the rectified voltage.

Illustration 4

Diodes are connected in the circuits as shown. Find their biasing with the data given :

(a) 

(b) 

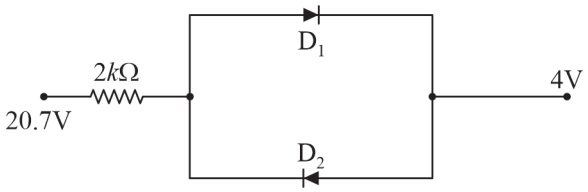
SOLUTION :

(a) p-side of the diode is at higher potential and so it is in FB.

(b) RB.

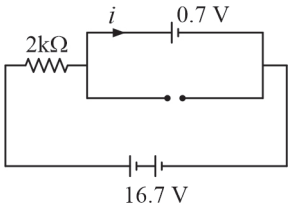
Illustration 5

Determine the current 1 in the circuit shown in figure. Assume diodes are made of siicon (V_0 = 0.7 V).



SOLUTION :

In the given circuit, D_1 is in FB and D_2 is in RB and so current will pass through D_1.

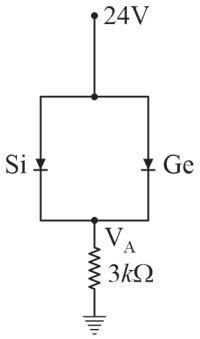


The equivalent circuit is :

Current $i = \dfrac{16.7 - 0.7}{2 \times 10^3} = 8 \times 10^{-3}\, A = 8\, mA$

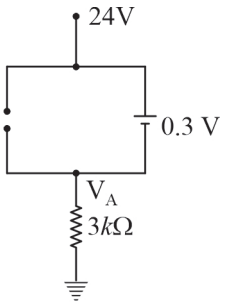
Illustration 6

Find the voltage V_A is the circuit shown in figure. The potentia barrier for Ge is 0.3 V and for Si is 0.7 V.



SOLUTION :

In the situation given, germanium diode will turn on first because potential barrier for germanium is smaller. The silicon diode wil not get the opportunity to flow the current and so remains in open circuit. The equivalent circuit is as in figure.

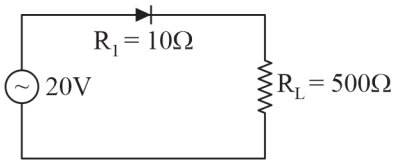


$V_A = 24 - 0.3$

$= 23.7$ V

Illustration 7

An ac voltage of peak value 20 V is connected in series with silicon diode and a load resistance of 500 Ω. The forward resistance of the diode is 10 Ω and the barrier voltage is 0.7 V. Find the peak current through diode and the peak voltage across the load. What will happen to these values if the diode is assumed to be ideal.



SOLUTION :

The diode will be in forward bias only in positive half cycle of ac. As potential barrier of diode is 0.7 V and so net peak potential of the circuit becomes 20 – 0.7 V = 19.3 V. Given load resistance R_L = 500 Ω, and R_f = 10 Ω.

$\therefore$ Peak current $i = \dfrac{\text{net peak potential}}{\text{total assistance}} = \dfrac{19.3}{500 + 10} = 0.038\, A$

The peak voltage across the load resistor = $i\, R_L = 0.038 \times 500 = 18.9$ V

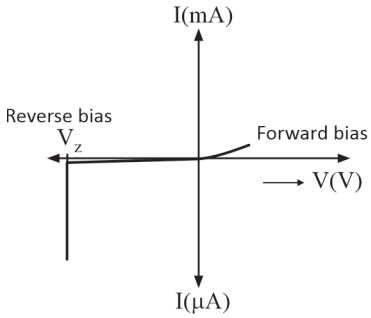
For idea diode R_f becomes zero and so barrier potential also becomes zero. Thus

peak current $i' = \frac{20}{500} = 0.04A$ and peak potential = 20 V

Special Purpose p-n Junction Diodes :

I. Zener Diode :

- It is a special purpose semiconductor diode designed to operate under reverse bias in the breakdown region and used as a voltage regulator.



I-V characteristics of zener diode

- Zener diode is fabricated by heavily doping both p– and n-side of the junction due to which, the depletion region formed is very thin and the electric field in the junction is extremely high ($\sim 5 \times 10^{-6}$ Vm^{-1}) even for a small reverse bias voltage of about 5V.
- When the applied reverse bias voltage (V) reaches the breakdown voltage (V_z) of the Zener diode, there is a large change in the current.

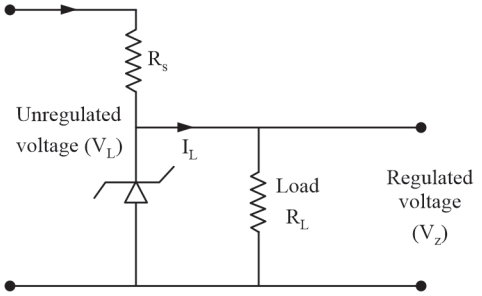
  Let us understand how reverse current suddenly increases at the breakdown voltage.
- We know that reverse current is due to the flow of electrons (minority carriers) form p → n and holes from n → p.
- As the reverse bias voltage is increased, the electric field at the junction becomes significant.
- When the reverse bias voltage $V = V_z$, then the electric field strength is high enough to pull valence electrons from the host atom on the p -side which are accelerated to n – side. These electrons account for high current observed at the breakdown.
- The emission of electrons from the host atoms due to the high electric field is known as internal field emission or field ionization.
- After the breakdown voltage V_z, a large change in the current can be produced by almost insignificant change in the reverse bias voltage.

  In other words, Zener Voltage remain constant, even though current through the Zener diode varies over a wide range.

  This property of the Zener diode is used for regulating supply voltages so that they are constant.

Zener Diode as a Voltage Regulator :

To get a constant dc voltage from the dc unregulated output of a rectifier, we use a zener diode.



Zener diode as DC voltage regulator

MORE TO KNOW

In general, current through Zener diode (I_z) should be sufficiently larger than current through load (I_L) (eg : $I_Z \approx 5I_L$)

Working :

- The unregulated dc voltage (filtered output of a rectifier) is connected to the Zener diode through a series resistance R_s such that the Zener diode is reverse biased.
- If the input voltage increases, the current through R_s and Zener diode also increases. This increases the voltage drop across R_s without any change in the voltage across the Zener diode.
- This is because in the breakdown region, Zener voltage remains constant even though the current through the Zener diode changes.
- Similarly, if the input voltage decreases, the current through R_s and Zener diode also decreases. The voltage drop across R_s decreases without any change in the voltage across the Zener diode.
- Thus, any increase/decrease in the input voltage results in, increase/decrease of the voltage drop across R_s without any change in voltage across the Zener diode.

Thus, the zener diode acts as a voltage regulator.

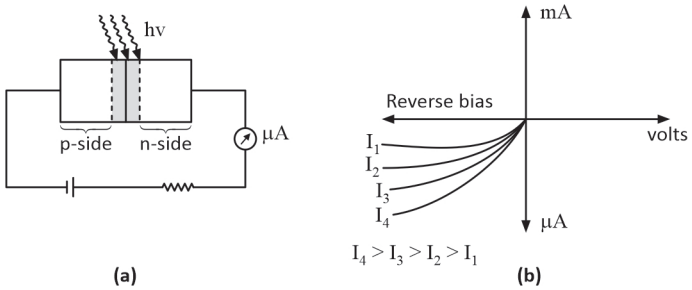
II. Optoelectronic Junction Devices :

(a) *Photodiodes* used for detecting optical signal (photo detectors)

(b) *Light Emitting Diodes* (LED) which convert electrical energy into light.

(c) *Photovoltaic devices* which convert optical radiation into electricity (solar cells).

(a) Photodiode :



(a) An illuminated photodiode under reverse bias,

(b) I - V characteristics of a photodiode for different intensity $I_4 > I_3 > I_2 > I_1$

- A photodiode is a special purpose p-n junction diode operated under reverse bias and is fabricated with a transparent window to allow light to fall on the diode.
- When the photodiode is illuminated with light (photons) with energy ($h\nu$) greater than the energy gap (E_g) of the semiconductor, then electron – hole pairs are generated due to the absorption of photons.
- The diode is fabricated such that the generation of e-h pair takes place in or near the depletion region of the diode.
- Due to electric field of the junction, electrons and holes are separated before they recombine. The direction of the electric field is such that electrons reach n-side and holes reach p-side.
- Electrons are collected on n-side and holes are collected on p-side giving rise to an emf. When an external load is connected, current flows.

Practice Question **:**

The current in the forward bias is known to be more (~mA) than the current in the reverse bias (~μA). What is the reason then to operate the photodiodes in reverse bias?

Ans : The fractional change due to the photo effects on the minority carrier dominated reverse bias current is more easily measurable than the fractional change in forward bias current. Hence, photodiode are preferably used in the reverse bias condition for measuring light intensity.

E.g.: In n-type semi-conductor, $Q >> K$ At any illumination,

c Q Q'

c Q such that $\Delta Q = \Delta K$? (Majority carrier) $\frac{\Delta}{} <<< \frac{\Delta Q}{Q}$ $\frac{K}{K}$ (minority carrier)

Note**:** The magnitude of photocurrent depends on the intensity of incident light. (Photocurrent is proportional to incident light intensity).

(b) Light Emitting Diode:

It is a heavily doped p-n junction which under forward bias emits spontaneous radiation. The diode is encapsulated with a transparent cover so that emitted light can come out.

When the diode is forward biased, electrons are sent from n → p (where they are minority carriers) and holes are sent from p → n (where they are minority carriers).

At the junction boundary, the concentration of minority carriers increases compared to the equilibrium concentration (i.e., when there is no bias). Thus, at the junction boundary on either side of the junction, excess minority carriers are there which recombine with majority carriers near the junction.

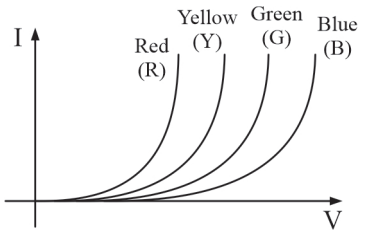
On recombination, the energy is released in the form of photons. Photons with energy equal to or slightly less than the band gap are emitted.

When the forward current of the diode is small, the intensity of light emitted is small. As the forward current increases, intensity of light increases and reaches a maximum. Further increase in the forward current results in decrease in light intensity. LEDs are biased such that the light emitting efficiency is maximum.

The semiconductor used for fabrication of visible LEDs must at least have a band gap of 1.8 eV (spectral range of visible light is from about 0.4 μm to 0.7 μm, i.e. from about 3eV to 1.8 eV). GaAs (Eg ~ 1.4eV) used for making infrared LED.

Uses : The LEDs find extensive use in remote controls, burglar alarm systems, optical communication, etc.

LEDs have the following advantages over conventional incandescent low power lamps :



(i) Low operational voltage and less power.

(ii) Fast action and no warm-up time required.

(iii) The bandwidth of emitted light is 100 Å to 500 Å or in other words it is nearly (but not exactly) monochromatic.

(iv) Long life and ruggedness.

(v) Fast on-off switching capability.

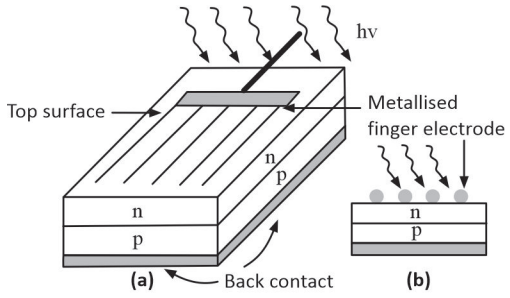
(c) Solar Cell :

Definition :

(i) A solar cell is basically a p-n junction which generates emf when solar radiation falls on the p-n junction.

(ii) It works on the same principal (photovoltaic effect) as the photodiode, except that no external bias is applied and the junction area is kept much larger for solar radiation to be incident because we are interested in more power.

➤ **Construction :**



(a) Typical p - n junction solar cell
(b) Cross - sectional view.

(a) A *p* – S*i* wafer of about 300 μ*m* is taken over which a thin layer (~0.3 μ*m*) of n-Si grown on one-side by diffusion process. ('n' is thin so that light can reach junction (depletion region))

(b) The other side of *p*-S*i* is coated with a metal (back contact).

(c) On the top of *n*-S*i* layer, metal finger electrode (or metallic grid) is deposited. This acts as a front contact.

(d) The metallic grid occupies only a very small fraction of the cell area (< 15%) so that light can be incident on the cell from the top.

➤ **Working :**

The generation of emf by a solar cell, when light falls on it, is due to the following three basic process :

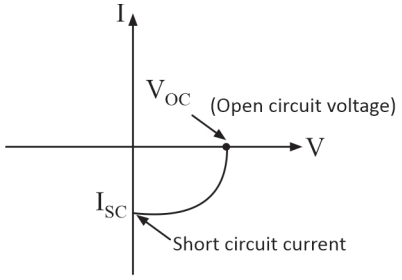
(i) ***Generation*** **:** generation of e – *h* pairs due to light (with $hv > E_g$) close to the junction ;

(ii) ***Separation*** **:** separation of electrons and holes due to electric field of the depletion region. Electrons are swept to *n*-side and holes to p-side ;

(iii) ***Collection*** **:** the electrons reaching the n-side are collected by the front contact and holes reaching p-side are collected by the back contact.

Thus, *p*-side becomes positive and n-side becomes negative giving rise to *photovoltage*.

❒ **Criteria for the selection of material for Solar Cell Fabrication :**



I - V characteristics of a solar cell.

- ➤ Band gap (~ 1.0 to 1.8 eV) (close to 1.5 eV are ideal for solar cell fabrication)
- ➤ High optical absorption (~ $10^4\, cm^{-1}$)
- ➤ Electrical conductivity
- ➤ Availability of the raw material
- ➤ Cost

Practice Question **:**

The I-V curve of Solar cell lies in the 4th Quadrant. Explain.

Ans: Here current flow is like reverse biased (from $n \rightarrow p$) & potential difference is like Forward Biased ('*p*' is +ve & '*n*' $-ve$) (because No external biasing). Thus I – V graph lies in 4th Quadrant.

Note **:** Sunlight is not always required for a solar cell. Any light with photon energies greater than the band gap will do.

Uses : Solar cells are used to power electronic devices in satellites and space vehicles and also as power supply to some calculators.

Junction Transistor :

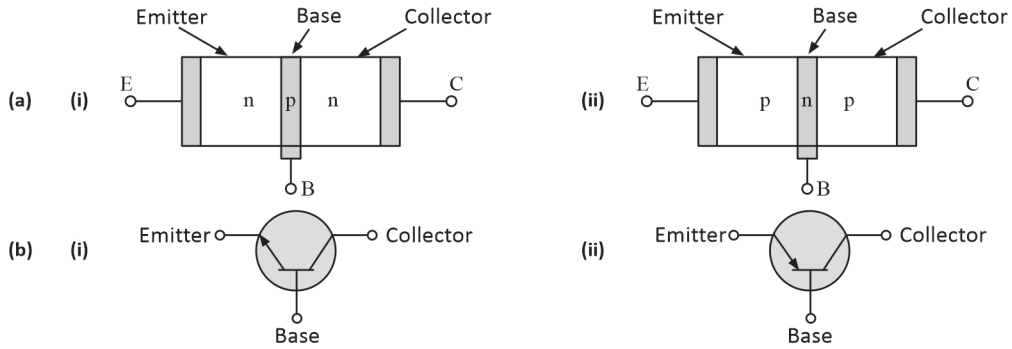
I. Transistor - Structure and Action :

The transistor consists of two *p*-*n* junctions back to back and is obtained by sandwiching either *p*-type or *n*-type semiconductor between a pair of opposite type semiconductors.

There are two types of semiconductors:

(i) *n-p-n transistor* : Here two segments of *n*-type semiconductor (emitter and collector) are separated by a segment of *p*-type semiconductor (base).

(ii) *p-n-p transistor* : Here two segments of *p*-type semiconductor (termed as emitter and collector) are separated by a segment of *n*-type semiconductor (termed as base).

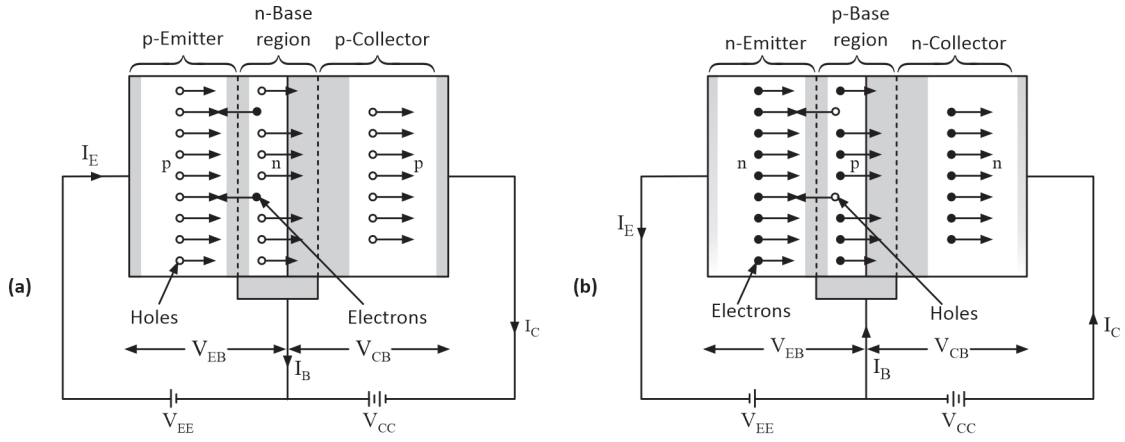


(a) Schematic representations of a n-p-n transistor and p-n-p transistor, and
(b) Symbols for n-p-n and p-n-p transistors.

Note **:** All the three segments of a transistor have different thickness and their doping levels are also different.

The three segments of a transistor are :

- ***Emitter*** **:** It is of moderate size and heavily doped. It supplies a large number of majority carriers for the current flow through the transistor.
- ***Base*** **:** This is the central segment. It is very thin and lightly doped.
- ***Collector*** **:** This segment collects of a major portion of the majority carriers supplied by the emitter. The collector side is moderately doped and larger in size as compared to the emitter.



Bias Voltage applied on : (a) p-n-p transistor and **(b)** n-p-n transistor.

The transistor works as an amplifier, with its emitter-base junction forward biased and the base-collector junction reverse biased.

We represent the voltage between emitter and base as V_{EB} and that between the collector and the base as V_{CB}.

If base is a common terminal for the two power supplies whose other terminals are connected to emitter and collector, respectively, the two power supplies are represented as V_{EE} and V_{CC} respectively.

In circuits, where emitter is the common terminal, the power supply between the base and the emitter is represented as V_{BB} and that between collector and emitter as V_{CC}.

The paths of current carriers in the transistor with emitter-base junction forward biased and base-collector junction reverse biased :

- The heavily doped emitter has a high concentration of majority carriers, which will be holes in a *p-n-p* transistor and electrons in an *n-p-n* transistor.
- These majority carriers enter the base region in large numbers. The base is thin and lightly doped. So the majority carriers there would be few. In a *p-n-p* transistor the majority carriers in the base are electrons since base is of *n*-type semiconductor. The large number of holes entering the base from the emitter swamps the small number of electrons there.
- As the base-collector junction is reverse-biased, these holes, which appear as minority carriers at the junction, can easily cross the junction and enter the collector. The holes in the base could move either towards the base terminal to combine with the electrons entering from outside or cross the junction to enter into the collector and reach the collector terminal.

The base is made thin so that most of the holes find themselves near the reverse-biased base-collector junction and so cross the junction instead of moving to the base terminal.

- Due to forward bias a large current enters the emitter-base junction, but most of it is diverted to adjacent reverse-biased base-collector junction and the current coming out of the base becomes a very small fraction of the current that entered the junction.
- The *emitter current*, $I_E = I_h + I_e$ (where I_h and I_e represent the hole and the electron current crossing the forward biased diode) but the *base current*, $I_B << I_h + I_e$, because a major part of I_E goes to collector instead of coming out of the base terminal. The base current is thus a small fraction of emitter current.

  The current entering into the emitter form outside is equal to the emitter current I_E.

  Similarly, I_B : the current emerging from the base terminal

  I_C : the current emerging from the collector terminal

  By the application of Kirchoff's law, we have $I_E = I_C + I_B$

  i.e. the emitter current is the sum of collector current and base current.

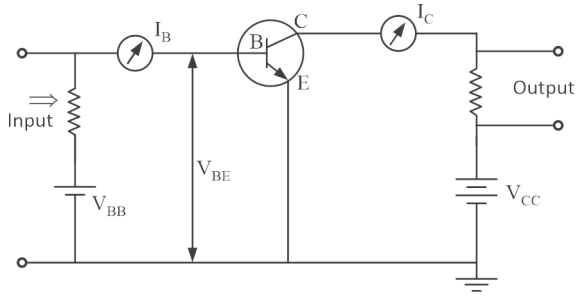
***Note*:** **(i)** In a p-n-p transistor, the current enters from emitter into base whereas in a n-p-n transistor it enters from the base into the emitter.

(ii) In the active state of the transistor, the emitter-base junction acts as a low resistance while the base-collector junction acts as a high resistance.

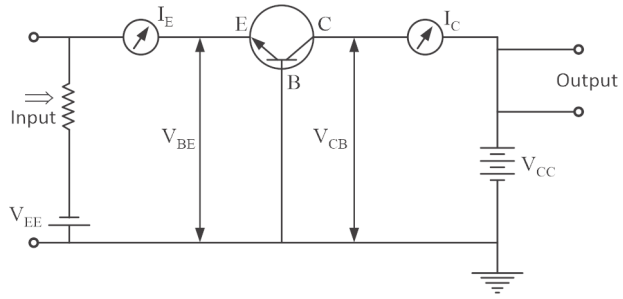
II. Basic Transistor Circuit Configurations and Transistor Characteristics :

In a transistor, only three terminals are available, viz., *Emitter* (E), *Base* (B) and *Collector* (C). Therefore, in a circuit the input/output connections have to be such that one of these (E, B or C) is common to both the input and the output. Accordingly, the transistor can be connected in either of the following three configurations :

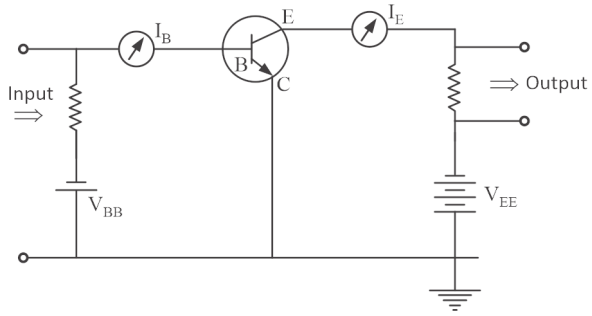
1. Common Emitter (CE) :



2. Common Base (CB) :

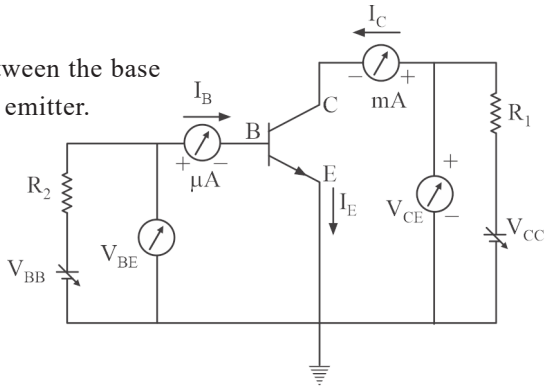


3. Common Collector (CC) :



Common Emitter Transistor Characteristics :

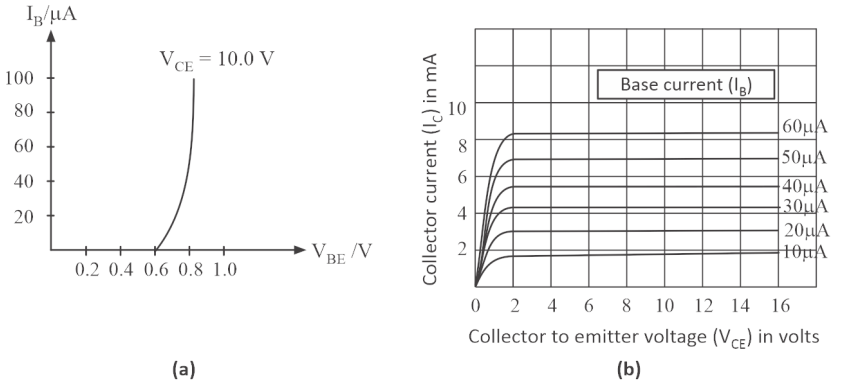
- When a transistor is used in CE configuration, the input is between the base and the emitter and the output is between the collector and the emitter.
- Input Characteristics:
  - The variation of the base current I_B with the base-emitter voltage V_{BE} is called input characteristic.
  - To study the input characteristics of the transistor in CE configuration, a curve is plotted between the base current I_B against the base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}.



Circuit arrangement for studying the input and output characteristics of n-p-n transistor in CE configuration

Note **:** We know, $V_{CE} = V_{CB} + V_{BE}$

Since the increase in V_{CE} appears as increase in V_{CB}, its effect on I_B is negligible. As a result, input characteristics for various values of V_{CE} will give almost identical curves. Hence, it is enough to determine only one input characteristics.



(a) Typical input characteristics and **(b)** Typical output characteristics

❒ Output Characteristics :

- The variation of the collector current I_C with the collector-emitter voltage V_{CE} at constant I_B is called the output characteristic.
- If V_{BE} is increased by a small amount, both hole current from the emitter region and the electron current from the base region will increase. As a consequence, both I_B and I_C will increase proportionately. This shows that when I_B increase, I_C also increases.
- The plot of I_C versus V_{CE} for different fixed values of I_B gives one output characteristic.

Some Important ac Parameters of Transistors :

1. Input resistance (r_i) :

This is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector emitter voltage (V_{CE}).

$$r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}}$$

{Of the order of a few "$k\Omega$" though ΔI_B is large with a small change in ΔV_{BE} because ΔI_B is of the order of "μA"}

Of the order of a few "$k\Omega$" though ΔI_B is large with a small change in ΔV_{BE} because is of the order of "μA".

2. Output resistance (r_o) :

This is defined as the ratio of change in collector emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant base current I_B.

$$r_o = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$$

{Of the order of "MΩ" because $\Delta I_C \approx 0$ (very less)}

Of the order of "$M\Omega$" because $\Delta I_C \approx 0$ (very less)

3. Current amplification factor (β) :

This is defined as the ratio of the change in collector current (output current) to the change in base current at a constant collector-emitter voltage (V_{CE}) when the transistor is the active state.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

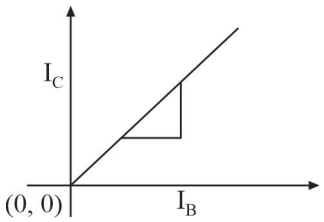
Thus is also known as Small Signal Current Gain.

Note : ➤ The output characteristics show that initially for very small values of V_{CE} , I_C increases almost linearly. This happens because the base-collector junction is not reverse biased and the transistor is not in active state.

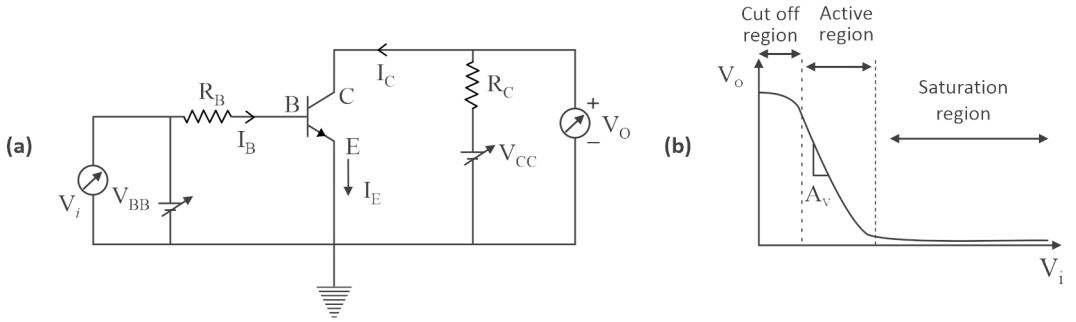
➤ The output resistance of the transistor is mainly controlled by the bias of the base-collector junction.

➤ β_{dc} of transistor $= \frac{I_C}{I_B}$

Since I_C increases with I_B almost linearly and $I_C = 0$ when $I_B = O$, the values of both β_{dc} and β_{ac} are nearly equal. So, for most calculations β_{dc} can be used. (Since slope is same, $\frac{\Delta I_B}{\Delta I_C} = \frac{I_{B-0}}{I_{C-0}}$ considering origin as one point. $\therefore B_{ac} \approx B_{dc}$ Numerically)



III. Transistor as a Switch :



(a) Base-biased transistor in CE configuration **(b)** Transfer characteristic

Principle:

(i) Applying Kirchhoff's voltage rule to the input and output sides of this circuit, we get :

$$V_{BB} = I_B R_B + V_{BE} \quad \text{and} \quad V_{CE} = V_{CC} - I_C R_C.$$

We shall treat V_{BB} as the dc input voltage V_i and V_{CE} as the dc output voltage V_O. So, we have

$$V_i = I_B R_B + V_{BE} \quad \text{and} \quad V_O = V_{CC} - I_C R_C.$$

(ii) In the case of Si transistor, as long as input V_i is less than 0.6 V, the transistor will be in cut off state and current I_C will be zero.

Hence $V_O = V_{CC}$

When V_i becomes greater than 0.6 V, the transistor is in active state with some current I_C in the output path and the output V_O decrease as the term $I_C R_C$ increases. With V_i, I_C increases almost linearly and so V_O decreases linearly till its value becomes les than about 1.0 V.

Beyond this, the change becomes non linear and transistor goes into saturation state. With further increase in V_i the output voltage is found to decrease further towards zero though it may never become zero.

Working :

As long as V_i is low and unable to forward-bias the transistor, V_0 is high (at V_{CC}).

If V_i is high enough to drive the transistor into saturation, then V_O is low, very near to zero.

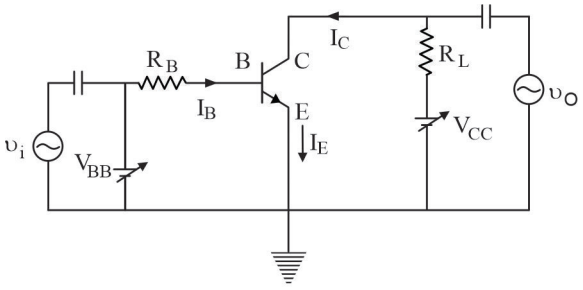
When the transistor is not conducting it is said to be *switched off* and when it is driven into saturation it is said to be *switched on*.

This shows that if we define low and high states as below and above certain voltage levels corresponding to cutoff and saturation of the transistor, then we can say that a low input switches the transistor off and a high input switches it on. Alternatively, we can say that a low input to the transistor gives a high output and a high input gives a low output.

The switching circuits are designed in such a way that the transistor does not remain in active state.

IV. Transistor as an Amplifier (CE-configuration) :

If a small sinusoidal voltage with amplitude v_s is superposed on the dc base bias by connecting the source of that signal in series with the V_{BB} supply, then the base current will have sinusoidal variations superimposed on the value of I_B. As a consequence the collector current also will have sinusoidal variations superimposed on the value of I_C producing in turn corresponding change in the value of V_O. We can measure the ac variations across the input and output terminals by blocking the dc voltages by large capacitors.



A simple circuit of a CE - transistor amplifier

Working :

Let us superimpose an ac input signal v_i (to be amplified) on the bias V_{BB} (dc).

The output is taken between the collector and the ground.

Let us assume that $v_i = O$

Then, applying Kirchhoff's law to the output loop, we get

$$V_{CC} - I_C R_L - V_{CE} = 0 \quad \Rightarrow \quad V_{CC} = I_C R_L + V_{CE} \quad \textbf{....(i)}$$

Likewise, the input loop gives

$$V_{BB} - I_B R_B - V_{BE} = 0 \quad \Rightarrow \quad V_{BB} = I_B R_B + V_{BE} \quad \textbf{....(ii)}$$

When v_i is not zero, we get :

$$V_{BB} + v_i = V_{BE} + \Delta_{BE} + (I_B + \Delta I_B) R_B \quad \Rightarrow \quad V_{BB} + v_i = V_{BE} + I_B R_B + \Delta I_B (R_B + r_i) \quad \textbf{....(iii)}$$

$\left[r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B} \right)_{V_{CE}} \right]$, where r_i is the input resistance

Hence, $v_i = \Delta I_B (R_B + r_i) = \Delta I_B \cdot r$

The change in I_B causes a change in I_C.

$$\beta_{ac} = \frac{\Delta V_C}{\Delta I_B} = \frac{i_C}{i_B} \qquad \text{....(iv)}$$

It is also know as the ac current gain A_i. Usually β_{ac} is close to β_{dc} in the linear region of the output characteristics. The change in I_C due to a change in I_B causes a change V_{CE} and the voltage drop across the resistor R_L because V_{CC} is fixed.

These changes can be give by $\Delta V_{CC} = \Delta V_{CE} + R_L \Delta I_C$ [Using Equation (i)]

$\Rightarrow \quad 0 = \Delta V_{CE} + R_L \Delta I_C \qquad \Rightarrow \qquad \Delta V_{CE} = -R_L \Delta I_C$

The change in V_{CE} is the output voltage v_0.

So, $v_0 = \Delta V_{CE} = -R_L \Delta I_C \qquad \Rightarrow \qquad v_0 = -\beta_{ac} R_L \Delta I_B$ [Using Equation (iv)]

The voltage gain of the amplifier is $A_v = \frac{v_0}{v_i} = \frac{\Delta V_{CE}}{r \Delta I_B} \Rightarrow A_v = -\frac{B_{ac} R_L}{r}$

Note : (The negative sign represents that output voltage is opposite in phase with the input voltage.

The power gain A_p can be expressed as the product of the current gain and voltage gain.

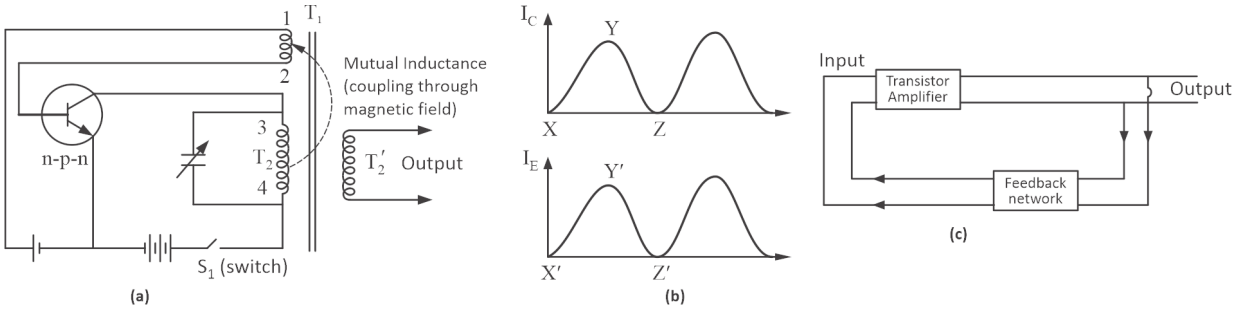
Mathematically, $A_p = \beta_{ac} \times A_v$

Since βac and Av are greater than 1, we get ac power gain. However, it should be realized that transistor is not a power generating device. The energy for the higher ac power at the output is supplied by the battery.

Transistor as an Oscillator :

In an oscillator, the output is *self sustained* which is accomplished by returning a portion of the output power to the input in phase with the starting power (This is called *positive feedback*).

Consider the circuit in which feedback is obtained by *inductive coupling*.



(a) Tuned collector oscillator, **(b)** Rise and fall (or built up) of current I_c and I_e due to the inductive coupling
(c) Principle of a transistor amplifier with positive feedback working as an oscillator

MORE TO KNOW

When first time S_1 is closed, reverse biasing is provided and current tries to shoot but because of inductor, current doesn't shoot rapidly and increases slowly. As a result flux increases through T_2 and corresponding EMF is induced in T_1 which provides forward biasing (increases forward biasing) and thus emitter current increases till Y' (saturation point). At saturation, collector current becomes const. and extra biasing provided by T_1 vanishes and thus emitter current decreases as a result collector current. Now, due to the decreases in collector current, emf is induced in T_1 but this time in opposite direction, as a result Forward biasing and emitter current further decreases till z'. This process continuous.

Working :

1. When the switch S_1 is put *on* to apply proper bias for the first time, a surge of collector current flows in the transistor. This current flows through the coil T_2 where terminals are numbered 3 and 4.
2. The current increases from *X* to *Y* (shown in Figure). The inductive coupling between coil T_2 and coil T_1 now causes a current to flow in the emitter circuit (this is the actual feedback).
3. As a result the current in T_1 (emitter current) also increases from *X'* to *Y'*.
4. The current in T_2 (collector current) connected in the collector circuit acquires the value *Y* when transistor becomes saturated *i.e.* maximum collector current is flowing and can increase no further.
5. Since there is no further change in collector current, the magnetic field around T_2 ceases to grow. As soon as the field becomes static, there will be no further feedback from T_2 to T_1. Without continued feedback, emitter current begins to fall. Consequently, collector current decreases from *Y* towards *Z*.
6. However, a decrease of collector current causes the magnetic field to decay around coil T_2. Thus, T_1 is now seeing a decaying field in T_2. This causes a further decrease in the emitter current till it reaches *Z* when transistor is cut-off. The whole process repeats itself.
7. The frequency at which the oscillator oscillates is given by $f = \frac{1}{2\pi\sqrt{LC}}$

   In this current, the tank or tuned circuit is connected in the collector side and it is known as *tuned collector circuit*.

Illustration 8

Find the value of b if (i) $\alpha = 0.9$ (ii) $\alpha = 0.99$

SOLUTION :

We know that $\beta = \frac{\alpha}{1-\alpha} = \frac{0.9}{1-0.9} = 9$

and $\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$

Illustration 9

Calculate the emitter current I_E in a transistor for which $\beta = 50$ and $i_B = 20\ \mu A$.

SOLUTION :

We know that $\beta = \frac{i_C}{i_B}$

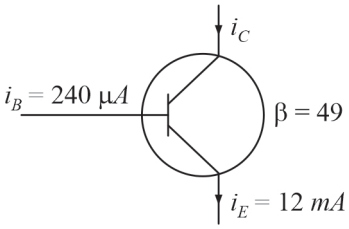
$\therefore \quad i_C = \beta\, i_B = 50 \times 0.02 = 1\ mA$

Emitter current $i_E = i_B + i_C = 0.02 + 1 = 1.02\ mA$

Illustration 10

Find the value of i_C and α from the data given in the figure.

SOLUTION :



We know that $i_E = i_B + i_C$

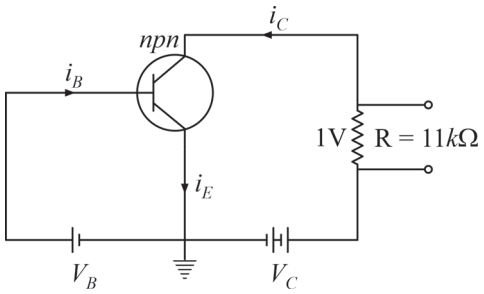
$i_C = i_E - i_B$

$= 12 - 0.24 = 11.76$ mA

Current gain $\alpha = \dfrac{\beta}{1+\beta} = \dfrac{49}{1+49} = 0.98$

Illustration 11

For a transistor, $\beta = 45$ and voltage drop across $1k\Omega$ which is connected in the collector circuit is 1 volt. Find the base current for common emitter connection.



SOLUTION :

From the data given,

$$i_C = \frac{1}{1\times10^3} = 10^{-3}\ A = 1\ mA$$

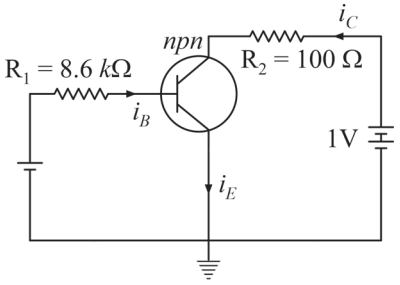
We know that,

$$\beta = \frac{i_C}{i_B}$$

$$\therefore \quad i_B = \frac{i_C}{\beta} = \frac{1}{45} = 0.022\ mA$$

Illustration 12

A silicon transistor amplifier circuit is given below :



If the current amplifier factor $\beta = 100$, determine :

(a) base current i_B **(b)** collector current i_C

(c) collector-emitter voltage **(d)** collector base-voltage

Take the voltage drop between base and emitter as 0.7 V.

SOLUTION :

(a) Figure represents npn transistor in common emitter connection.

Applying Kirchhoff's loop rule in base-emitter circuit.

$$+5 - i_B R_1 - V_{\text{barrier}} = 0$$

$$\therefore \quad i_B = \frac{5 - V_{barrier}}{R_1} = \frac{5-0.7}{8.6\times10^3} = 0.5\ mA$$

(b) We know that $\beta = \dfrac{i_C}{i_B}$

$$\therefore \quad i_C = \beta i_B = 100\times0.5 = 50\ mA$$

(c) Applying Kirchhoff's loop rule in collector-emitter circuit, we have

$$i_C R_2 - 10 + V_{CE} = 0$$

$$\therefore \quad V_{CE} = 10 - i_C R_2 = 10 - 50\times10^{-3}\times100 = 5\ \text{V}$$

(d) For collector-base, we can write

$$V_{CE} = V_{CB} + V_{BE}$$

$$\therefore \quad V_{CB} = V_{CE} - V_{BE} = 5 - 0.7 = 4.3\ \text{V}$$

Illustration 13

Find voltage gain and power gain in common-base amplifier.

SOLUTION :

If input and output resistance are R_1 and R_2 respectively, then

Voltage gain $A_v = \dfrac{\text{output voltage}}{\text{input voltage}} = \dfrac{i_C R_2}{i_E R_1} = \alpha \dfrac{R_2}{R_1}$

Power gain $= \dfrac{\text{output voltage}}{\text{input voltage}} = \dfrac{i_C^2 R_2}{i_E^2 R_1} = \alpha^2 \dfrac{R_2}{R_1}$

Digital Electronics and Logic Gates :

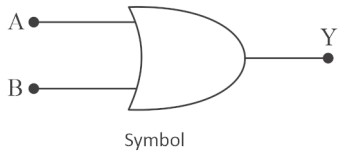
Analog Signals : The signals in the form of time-varying voltage or current are called Analog Signals.

Digital Signals : A signal having only 2 levels of voltage is called digital signal. In digital circuits, only two values (represented by 0 or 1) of the input and output voltage are permissible. 0 (say 0 V) and 1 (say 5 V) just like a light bulb if it is *on* we have 1 state and if it is *off* we have zero state.

Logic Gates : A gate is digital circuit that follows certain logical relationship between the input and output voltages. Therefore, they are generally known as *logic gates*-gates because they control the flow of information. The five common logic gates used are NOT, AND, OR, NAND, NOR. Each logic gate is indicated by a symbol and its function is defined by a *truth table* that shows all the possible input logic level combinations with their respective output logic level. Truth tables help understand the behaviour of logic gates.

1. **OR Gate :** An OR gate has two or more inputs with one output. The output Y is 1 when either input A or input B or both are 1s, i.e. if any of the input is high, the output is high.

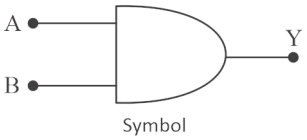
Truth Table		
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1



Symbol

2. **AND Gate :** An AND gate has two or more inputs and one output. The output Y of AND gate is 1 only when input A and input B are both 1.

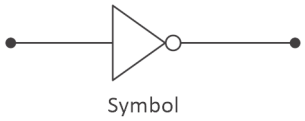
Truth Table		
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



Symbol

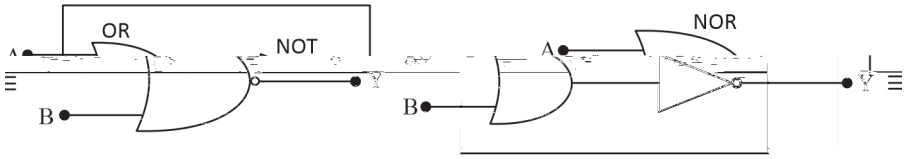
3. NOT Gate : This is the most basic gate, with one input and one output. It produces a '1' output if the input is '0' and vice-versa. That is, it produces an inverted version of the input at its output. This is way it is also known as an *inverter*.

Truth Table	
A	Y
1	0
0	1



4. NOR Gate : Combination of NOT gate and OR gate

It has two or more input and one output. A NOT – operation applied after OR gate gives a NOT – OR gate (or simply NOR gate). Its output Y is '1' only when both inputs A and B are '0', i.e., neither one input nor the other is '1'.



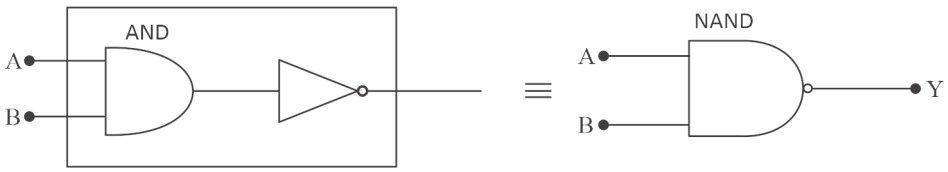
Replace the circuit diagram of OR and NOT gates to get circuit diagram of NOR

Truth Table		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NOR gates are considered as *universal gates* because you can obtain all the gates like AND, OR, NOT by using only NOR gates.

5. NAND Gate : Combination of AND and NOT gate

Nand gates are also called *Universal Gates* since by using these gates you can realise other basic gates like OR, AND NOT



NAND and NOR gates are called UNIVERSAL gates since by using these gates you can realize other gates like OR, AND and NOT.

Truth Table		
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Integrated Circuits (IC) :

An IC is the fabrication of an entire circuit consisting of passive components like R and C on a small single block of a semi conductor. The chip dimensions are as small as 1mm × 1mm or it could be even smaller.

Depending on nature of input signals, IC's can be grouped in two categories:

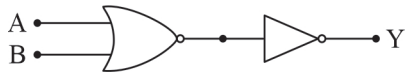
(a) ***Linear or Analogue IC's*****:** The linear IC's process analogue signals, which change smoothly and continuously over a range of values between a maximum and a minimum. The output is more or less directly proportional to the input, i.e., it varies linearly with the input.

One of the most useful linear IC's is the operational amplifier.

(b) ***Digital IC's*****: The** digital IC's process signals that have only two values. They contain circuits such as logic gates. Depending upon the level of integration (i.e., the number of circuit components or logical gates), the ICs are termed as Small Scale Integration, SSI (logic gates ≤ 10) ; Medium Scale Integration, MSI (logic gates ≤ 100) ; Large Scale Integration, LSI (logic gates ≤ 1000) ; and Very Large Scale Integration, VLSI (logic gates > 1000).

Illustration 14

By using NOR gate, construct OR gate.



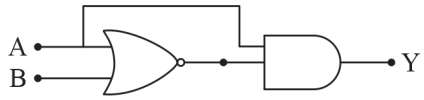
SOLUTION :

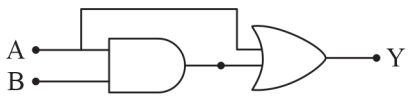
If output signal of NOR is sent into NOT gate, then final Output is equivalent to OR gate. Thus

$$\text{NOR} + \text{NOT} = \text{OR} + \text{NOT} + \text{NOT} \Rightarrow \text{OR}$$

Illustration 15

Write the truth table for the combination of gates as shown in figure.

(a) 

(b) 

SOLUTION :

(a)

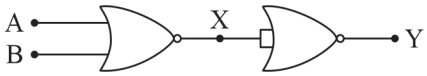
A	B	A + B	A.(A + B) = Y
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

(b)

A	B	A.B	A + (A.B)
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

Illustration 16

The output of an OR gate is connected to both the inputs of a NOR gate. Draw the logic circuit for this combination and write the truth table.



SOLUTION :

$$\frac{A+B=X}{(A+B)+(A+B)}=\overline{A+B}=Y$$

A	B	X	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

MICELLANEOUS EXERCISE

1. In intrinsic semiconductor at room temperature numbers of electrons and holes are:

(A) Unequal **(B)** Equal **(C)** Infinite **(D)** Zero

2. *P*-type semiconductors are made by adding impurity element.

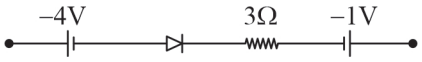
(A) *As* **(B)** *P* **(C)** *B* **(D)** *Bi*

3. Avalanche breakdown is due to :

(A) Collision of minority charged carrier **(B)** Increase in depletion layer thickness

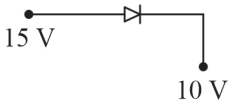
(C) Decrease in depletion layer thickness **(D)** None of these

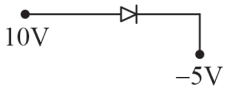
4. Find the magnitude of current in the circuit shown in the figure.



(A) Zero **(B)** 1 *amp* **(C)** 0.1 *amp* **(D)** 0.2 *amp*

5. Which is reverse biased diode?

(A)


(B)


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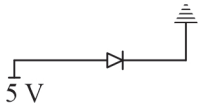

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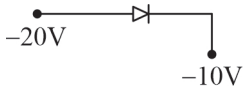
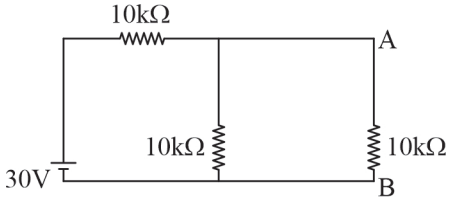


6. Charge density for intrinsic semiconductor will be :

(A) $15\times10^{17}\ m^{-3}$ **(B)** $1.6\times10^{16}\ m^{-3}$ **(C)** $5\times10^{13}\ m^{-3}$ **(D)** $15\times10^{14}\ m^{-3}$

7. Refer to the figure. Potential difference between *A* and *B* is :



(A) Zero **(B)** 5 *V* **(C)** 10 *V* **(D)** 15 *V*

8. Zener breakdown will occur if

(A) Impurity level is low **(B)** Impurity level is high

(C) Impurity is less in *K*-side **(D)** Impurity is less in *K*-side

9. In a *P*-*N* junction having depletion layer of thickness 10^{-6} *m* the potential across it is 0.1 *V*. the electric field is :

(A) 10^{7} **(B)** 10^{-6} **(C)** 10^{5} **(D)** 10^{-5}

10. Potential barrier developed in a junction diode opposes.

(A) Minority carries in both regions only **(B)** Majority carries

(C) Electrons in *N*-region **(D)** Holes in *P*-region

11. The process of adding impurities to the pure semiconductor is called.

(A) Drouping **(B)** Drooping **(C)** doping **(D)** None of these

12. In a *P*-*N* junction.

(A) *P* and *N* both are at the same potential

(B) High potential is at *N* side and low potential is at *P* side

(C) High potential is at *P* side and low potential is at *N* side

(D) Low potential is at *N* side and zero potential is at *P* side

13. On increasing the reverse bias to a large value in a *P*-*N* junction diode, the current.

(A) Remains fixed **(B)** Decreases slowly

(C) Increases slowly **(D)** Suddenly increases

14. The potential barrier, in the depletion layer, is due to :

(A) Ions **(B)** Holes **(C)** Electrons **(D)** Both **(B)** and **(C)**

15. At room temperature, a *P*-type semiconductor has :

(A) Large number of holes and few electrons **(B)** Large number of free electrons and a few holes

(C) Equal number of free electrons and holes **(D)** No electrons or hole

16. The valence band and conduction band of a solid overlap at low temperature. The solid may be :

(A) A metal **(B)** A semiconductor **(C)** An insulator **(D)** None of these

17. Which impurity is doped in *Si* to form *N*-type semiconductor?

(A) *Al* **(B)** *B* **(C)** *As* **(D)** None of these

18. In a semiconductor

(A) There are no free electrons at any temperature

(B) The number of free electrons is more than that in a conductor

(C) There are no free electrons at 0 *K*

(D) None of these

19. If n_p and n_c are the number of holes and electrons, then in an intrinsic semiconductor,

(A) $n_p > n_e$ **(B)** $n_p = n_e$ **(C)** $n_p < n_e$ **(D)** $n_p \neq n_e$

20. Donor type impurity is found in :

(A) Trivalent element **(B)** Pentavalent elements

(C) In both the above **(D)** None of these

21. In the middle of the depletion layer of a reverse-biased *P-N* junction, the :

(A) Potential is zero **(B)** Electric field is zero

(C) Potential is maximum **(D)** Electric filed is maximum

22. If a full wave rectifier circuit is operating from 50 Hz mains, the fundamental frequency in the ripple will be:

(A) 50 *Hz* **(B)** 70.7 *Hz* **(C)** 100 *Hz* **(D)** 25 *Hz*

23. The difference in the variation of resistance with temperature in a metal and a semiconductor arises essentially due to the difference in the :

(A) Variation of scattering mechanism with temperature **(B)** Crystal structure

(C) Variation of the number of charge carries with temperature **(D)** Type of bonding

24. A piece of copper and another of germanium are cooled from room temperature to 77 *K*, the resistance of :

(A) Each of them increases

(B) Each of them decreases

(C) Copper decreases and germanium increases

(D) Copper increases and germanium decreases

25. The manifestation of band structure in solids is due to :

(A) Heisenberg's uncertainty principle **(B)** Pauli's exclusion principle

(C) Bohr's correspondence principle **(D)** Botazmann's law

26. When a *P-N* junction diode is forward biased, then :

(A) The depletion region is reduced and barrier height is increased

(B) The depletion region is widened and barrier height is reduced

(C) Both the depletion region and barrier height are reduced

(D) Both the depletion region and barrier height are increased

27. When *npn* transistor is used as an amplifier :

(A) Electrons move from base to collector **(B)** Holes move from emitter to base

(C) Electrons move from collector to base **(D)** Holes move from base to emitter

28. For a transistor amplifier in common emitter configuration for load impedance of $1k\Omega$($h_{fe} = 50$ and $h_{oe} = 25$) the current gain is :

(A) –5.2 **(B)** –15.7 **(C)** –24.8 **(D)** –48.78

29. In an *NPN* transistor the collector current is 24 *mA*. If 80% of the electrons reach collector, its base current in *mA* is:

(A) 36 **(B)** 26 **(C)** 16 **(D)** 6

30. Choose the only false statement from the following.

(A) In conductors the valence and conductions bands overlap

(B) Substance with energy gap of the order of 10 *eV* are insulators

(C) The resistivity of a semiconductor increases with increase in temperature

(D) The conductivity of semiconductors increases with increase in temperature

31. Application of a forward bias to a *P-N* junction

(A) Widens the depletion zone

(B) Increases the potential difference across the depletion zone

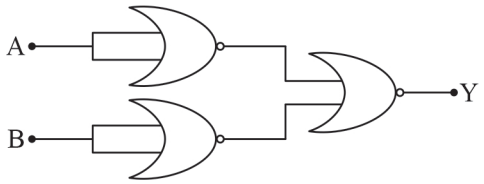
(C) Increases the number of donors on the *N* side

(D) Increase the electric field in the depletion zone

32. Carbon, silicon and germanium atoms have four valence electrons each. Their valence and conduction bands are separated by energy band gaps represented by $(E_g)_C$, $(E_g)_{Si}$ and $(E_g)_{Ge}$ respectively. Which one of the following relationships is true in their case?

(A) $(E_g)_C > (E_g)_{Si}$ **(B)** $(E_g)_C < (E_g)_{Si}$ **(C)** $(E_g)_C = (E_g)_{Si}$ **(D)** $(E_g)_C < (E_g)_{Ge}$

33. Identify the operation performed by the circuit given below :



(A) NOT **(B)** AND **(C)** OR **(D)** NAND

34. In a transistor the collector current is always less than the emitter current because :

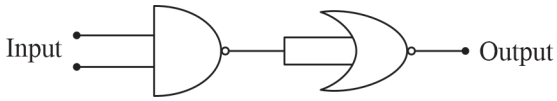
(A) Collector side is reverse biased and the emitter side is forward biased

(B) A few electrons are lost in the base and only remaining ones reach the collector

(C) Collector being reverse biased, attracts less electrons

(D) Collector side is forward biased and emitter side is reverse biased

35. The circuit given below represents which of logic operations?



(A) AND **(B)** NOT **(C)** OR **(D)** NOR

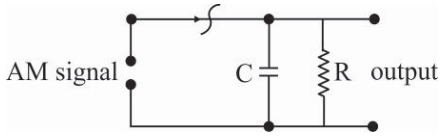
36. An amplifier has a voltage gain $A_V = 1000$. The voltage gain in *dB* is :

(A) 30 *dB* **(B)** 60 *dB* **(C)** 3 *dB* **(D)** 20 *dB*

37. A light emitting diode (*LED*) has a voltage drop of 2 volt across it and passes a current of 10 *mA* when it operates with a 6 volt battery through a limiting resistor *R*. The value of *R* is :

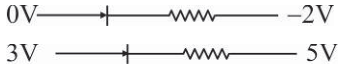
(A) 40 *k*Ω **(B)** 4 *k*Ω **(C)** 200 *k*Ω **(D)** 400 *k*Ω

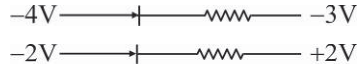
38. Given below is the circuit diagram of an *AM* demodulator. For good demodulation of *AM* signal of carrier frequency *f*, the value of *RC* should be :



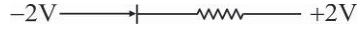
(A) $RC = 1/f$ **(B)** $RC < 1/f$ **(C)** $RC \geq 1/f$ **(D)** $RC >> 1/f$

39. A forward biased diode is :

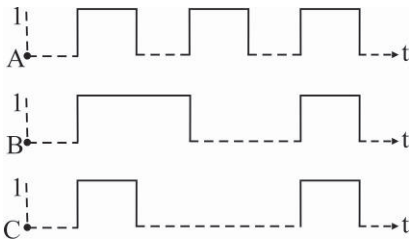
(A) 

(B) 

(C) 

(D) 

40. The following figure shows a logic gate circuit with two inputs A and B and the output C. The voltage waveforms of A, B and C are as shown below.



The logic circuit gate is :

(A) OR gate **(B)** AND gate **(C)** NAND gate **(D)** NOR gate

SOLUTIONS TO MICELLANEOUS EXERCISE

1.(B) At room temperature, in an intrinsic semiconductor Number of electrons (N_e) = number of holes (N_b).

2.(C) For P-type semiconductors, trivalent impurity should be added to intrinsic semiconductors which are tetravalent be elements. Hence boron = B should be added.

3.(A) Avalanche breakdown occurs on account of collision of minority charge carriers.

4.(A) It is a reverse bias diode.
P-crystal is given a potential = –4V ; N-crystal is given a potential = –1V
No current flows as P-crystal is more negative than N-crystal.

5.(B) In option (B)
P-crystal is at potential = – 20 V ; N-crystal is given a potential = – 10V
P crystal is more negative than N crystal.
P-N Nunction diode is reverse biased.

6.(B) For intrinsic semiconductor, Charge density $= 1.6\times10^{16}\ \text{m}^{-3}$

7.(C) Here P-N junction is forward biased. Resistance of ideal junction = zero.

$$R_{AB} = \frac{10\times10}{10+10} = \frac{10\times10}{20} = 5k\Omega = 5\times10^3\,\Omega$$

Current in circuit

$$(I) = \frac{Pd}{\text{Resistance}} = \frac{30}{(10+5)\times10^3} \quad \Rightarrow \quad I = \frac{2}{1000}\,\text{A}$$

$\therefore$ Current is equally divided in two equal resistance.

$\therefore$ Current in arm $AB = \frac{1}{2}\times\frac{2}{1000} = \frac{1}{1000}\text{A} \quad \Rightarrow \quad V_{AB} = \frac{1}{1000}\times\left(10\times10^3\right) = 10\text{V}$

8.(B) Zener breakdown occurs in highly droped P-N junction. Impurity means doping element.

9.(C) Intensity $(E) = \frac{P.d}{\text{distance}} = \frac{0.1}{10^{-6}} = 10^5\,\frac{V}{m}$

10.(B) Potential barrier developed in a junction diode opposes majority carriers only.

11.(C) Doping is the process of adding trivalent or pentavalent impurities to pure semi conductors which are tetravalent.

12.(B) In a P-N junction, high potential is N side and low potential is at P side.

13.(D) The current suddenly increases when reverse bias to a P-N junction is increased by large value.

14.(D) In a depletion layer, potential barrier is due to ions.

15.(A) In a P-type semiconductor, holes are majority charge carriers at room temperature.

16.(A) In metals, which are very good conductors of electricity, the valence band and the conduction band overlap.

17.(C) 'As' pentavalent.

18.(C) At 0 K, a semiconductor behaves as an insulator. There are no free electron available.

19.(B) $n_p = n_e$ in intrinsic semiconductors. Number of holes = number of electrons

20.(B) Pentavalent elements like arsenic can donate electrons. One pentavalent atom donates one electron.

21.(D) For a reverse biased P-N junction, electric field strength is maximum in the middle of depletion layer.

22.(C) In a full wave rectifier = 2 × input frequency

$\Rightarrow$ fundamental frequency = 2 × 50 $\Rightarrow$ fundamental frequency = 100 Hz.

23.(C) The number of charge carriers change with temperature. In semiconductors, carriers are more and so resistance is less as temperature increases. In metals, the situation is just reversed.

24.(C) Temperature falls from room temperature to 77 K. Hence resistance of metal / Cu decreases and that of germanium/ semiconductor increases.

25.(B) Pauli's exclusion principle is the cause of band structure of solids.

26.(C) Both the depletion region and barrier height are reduced when P–N junction diode is forward biased.

27.(A) When npn transistor is used as amplifier, majority charge carriers/electrons of n-type emitter travel from emitter to base and to collector.

28.(D) In common emitter configuration,

$$A_i = \frac{h_{fc}}{1 + h_{oe} \cdot R_L} \quad \Rightarrow \quad A_i = \frac{-50}{1 + \left(25 \times 10^{-6}\right) \times \left(1 \times 10^{3}\right)} = \frac{-50}{1.025}$$

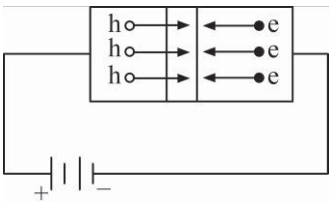
$$A_i = -48.78$$

29.(D) Since 80% of the electrons reach the collector, 20% only remain.

Base current $= \frac{20}{80} \times 24 = 6$ mA

30.(C) Resistivity of a semiconductor decreases with increase in the temperature.

31.(C) When battery is connected across P-N junction, more number of lectron enter in n side from battery which increases the number of donors on the N-side.



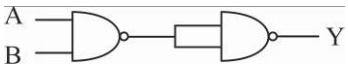
32.(A) Band gap of carbon is 5.5 eV while that of silicon is 1.1 eV.

$$(E_g)_C > (E_g)_{Si}$$

33.(B) $Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \,.\, \overline{\overline{B}} = A \,.B^*$

34.(B) $I_E = I_B + I_C \quad \therefore \qquad I_C < I_g$ A few electrons are lost to the base.

35.(A) $Y = \overline{\overline{A \cdot B}} = A \cdot B$



The given circuit is AND gate.

36.(B) Voltage gain in $dB = 20 \log 10\, A_V = 20 \log_{10}(1000) = 60$ B.

37.(D) As LED is connected to a battery through a resistance in series.
The current flowing, 10 mA is the same.
The voltage drop across LED = 2V

$\therefore$ As the battery has 6V, the potential difference across R = 4 V.

$$\therefore \qquad iR = 4V \;\Rightarrow\; R = \frac{4V}{10 \times 10^{-3}\ A} = 400\ \Omega$$

38.(D) For good demodulation, $\frac{1}{f} << RC$ or $RC >> \frac{1}{f}$.

39.(A) A diode is said to be forward biased if *P*-type semiconductor of *p-n* junction is at high potential with respect to *n*-type semiconductor of *P-N* junction. It is so for circuit.

40.(B) The truth table corresponding to waveform is given by :

A	B	C
1	1	1
1	0	1
1	0	0
0	0	0

$\therefore$ The given logic circuit gate is AND gate.